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# MS-7500 OB

BTX(264.16mm X 266.4mm)

## CPU:

AMD AM2R2+ Socket940

## System Chipset:

North Bridge --- AMD-ATI RX780/RS780

South Bridge --- AMD-ATI SB700

## OnBoard Chipset:

Clock Gen:Seligo P625

AZALIA Codec:ADI1884

LAN(PHY):BOARDCOM 5754 ( 5764 )

SIO:SMSC 5327

Flash ROM: 32 MB SPI (CHIP)

## Main Memory:

DDRII (667/800MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 1

## PWM:

Controller:ISL6323 ( 4-Phase 89W )

## ACPI:

INTERSIL 6545

## Other:

FDD \*1

SATA(SATA2-300MB/s) \*4

USB2.0 \*10 (Rear\*6 Front\*4)

DVI\*1

VGA PORT \*1

PRINT Header \*1

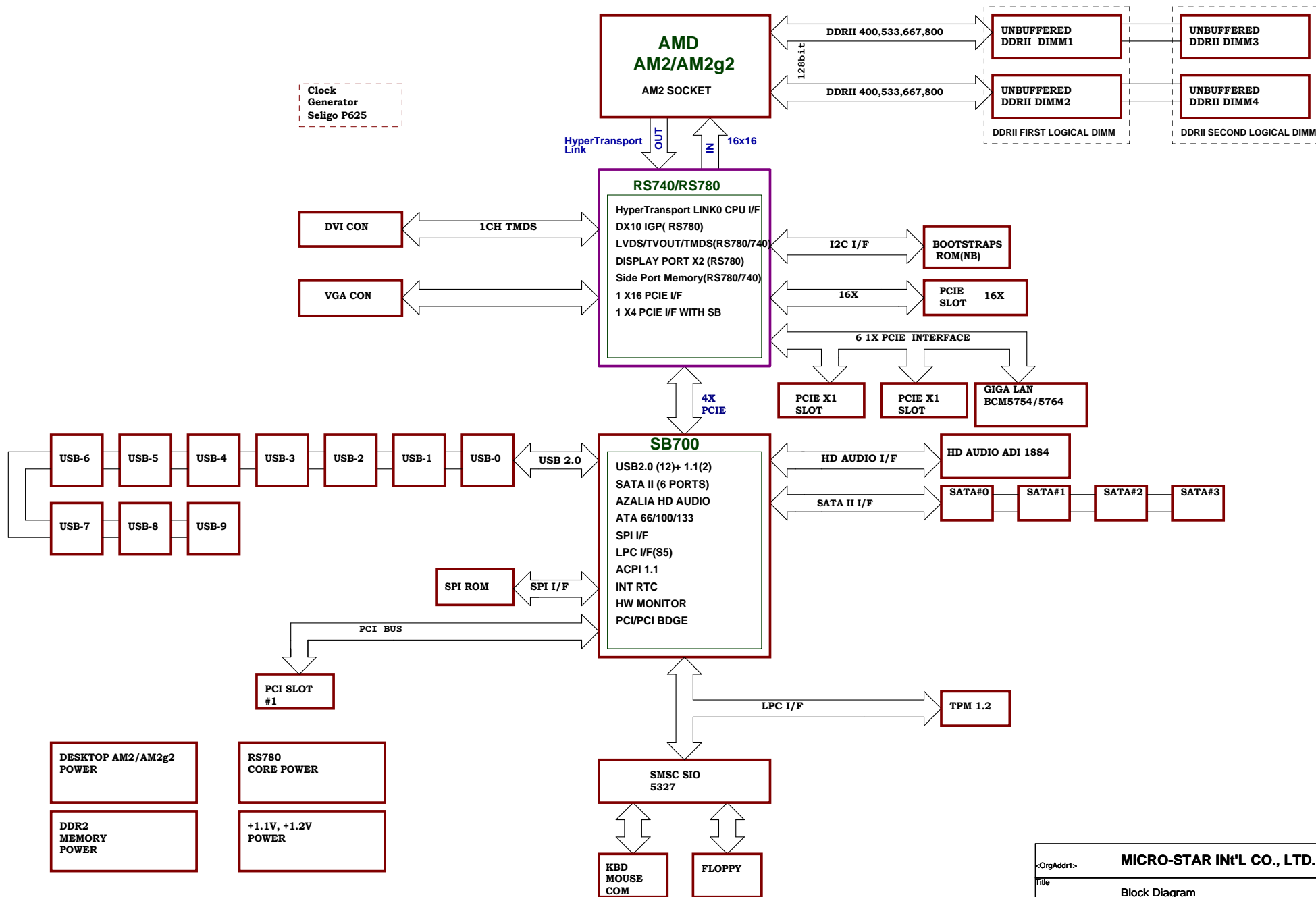
TPM \*1

COM PORT \*1

COM Header \*1

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## RX780/RS780 + SB700 CUSTOMER DESKTOP REFERENCE DESIGN



DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/−	OC#
Rear	QUAD STACK	USB0− USB0+ USB1− USB1+ USB2− USB2+ USB3− USB3+	USB_OC#0  ( OC#0~1 )
	LAN_USB1	USB4− USB4+ USB5− USB5+	USB_OC#1  ( OC#2 )
Front	FRONT USB	USB6− USB6+ USB7− USB7+	USB_OC#2  ( OC#3 )
	MEDIA CARD READER	USB8− USB8+ USB9− USB9+	USB_OC#3  ( OC#4 )

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD20	PCICLK2_SLOT1 (PCICLK2)
TPM				LPCCLK0
SIO				LPCCLK1

PCI RESET DEVICE

SB 700	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO

TABLE 37  
SIO8 GPIO ASSIGNMENTS

SIO GPIO	Function	Comment
GP 11	CHAFAN_PWM	Chassis Fan PWM command input, install 1K PU to +3.3 V
GP 12	RC_ID	Multi-state GPIO
GP 13	PME#	PME# from PCI slots.
GP 14	SMB Data Main	
GP 15	3V_SW_AUX	3V DUAL control
GP 16	WAKE#	PCI Express WAKE#, 1K PU to +3.3 V SB
GP 17	SMB_CLK_M	SMBus clock main
GP 21	DIAG_BEEP	Diagnostic beep signal; route to internal speaker amplifier
GP 22	CPUFAN_PWM	CPU Fan PWM command input, install 1K PU to +3.3 V
GP 23	AUDIO_AMP_DIS#	To disable internal speaker.

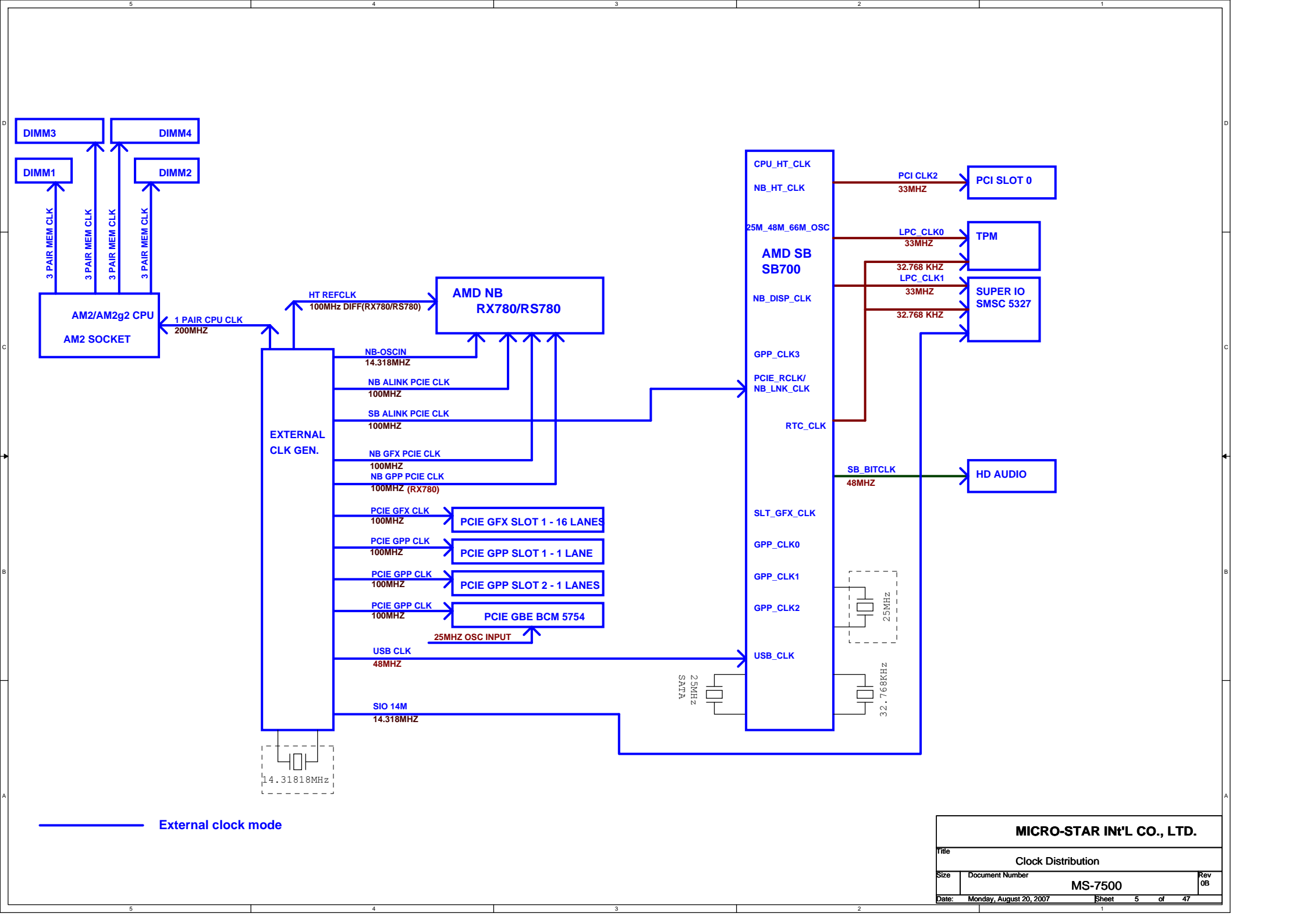
SIO GPIO	Function	Comment
GP 24	HOOD_SW_DET	Intrusion Switch Detect. Route to R126.1. Add 8.2K pullup to +3.3 V.
GP 25	HOOD_SENSE#	1M PU to SIO_BAT.
GP 26	SKTOCC#	Route to SKTOCC# on CPU, install 10M PU to BATT, CPU occupied signal
GP 27	WAKE_OUT#	Wake Disable Output.
GP 30	LED_COLOR	Route to P5.4, front LED/button header, power LED driver
GP 31	LED_BLINK	Route to P5.2, front LED/button header, power LED driver
GP 32	TRMTRIP#	Route to Thermtrip# voltage translation, 8.2K PU to +3.3 V, CPU shutdown
GP 33	HD_LED_IN#	Route to Hard Drive LED control circuit.
GP 36	SMBCLK_THERM	SMB clock for sensor bus for fan sense chip; 4.7K PU to + 3.3 V SB
GP 37	SMBDATA_THERM	SMB data for sensor bus for fan sense chip; 4.7K PU to + 3.3 V SB
GP 40	DENSEL#	Route to P10.2, floppy connector
GP 41	HD_LED_OUT#	Hard drive LED output
GP 42	RING#	Power management output to Southbridge Rtr# input, 8.2K PU to +3.3 V SB
GP 43	SMB_CLK_R	SMBus clock resume
GP 44	HOOD_LOCK#	Route to R124.1. install 2.2K pullup to +5 V
GP 45	HOOD_UNLOCK#	Route to R124.6. install 2.2K pullup to +5 V
GP 46	LPC_SMI#	LPC SMI output to Southbridge, install 8.2K pull up to +3.3 V SB
GP 50	RI2#	Route to 2 <sup>nd</sup> serial port RI# pin.
GP 51	DCD2#	Route to 2 <sup>nd</sup> serial port DCD# pin.
GP 52	RXD2	Route to 2 <sup>nd</sup> serial port RxDAT pin.
GP 53	TXD2	Route to 2 <sup>nd</sup> serial port TxDAT pin.
GP 54	DSR2#	Route to 2 <sup>nd</sup> serial port DSR# pin.
GP 55	RTS2#	Route to 2 <sup>nd</sup> serial port RTS# pin.
GP 56	CTS2#	Route to 2 <sup>nd</sup> serial port CTS# pin.
GP 57	DTR2#	Route to 2 <sup>nd</sup> serial port DTR# pin.
GP 60	CLAMP_CTRL	Clamp Control Signal. Route to power bleed off transistors.
GP 61	SIO_PCIE_RST#	Reset; route to PCI Express X1 and x16 slots
GP 62	PWRBTN_IN#	Front panel power button input
GP 63	SLP_S3#	Connected to S3 sleep input from Southbridge
GP 64	SLP_S4#	Connected to SLP_S4# (not S5) sleep input from Southbridge
GP 66	PWRBTN_OUT#	Route to Southbridge PWRBTN# input
GP 67	PSON#	Power supply main voltage control; route to P1.16, install 2.2K PU to +5 V_AUX
GP 70	USB_PWR#	Connected to SLP_S5#
GP 71	SMB DATA Resume	
GP 72	5V_DUAL_Control	Controls aux voltage FET on 5V_DUAL circuit
GP 73	CHAFAN2_TACH	Power supply tach input; 4.7K PU to +3.3 V
GP 74	CHAFAN2_PWM	Power supply PWM command input; 1K PU to +3.3 V
GP 75	PWRGD_30MS	Power Good delayed 30 ms. 1K PU to + 3 V SB
GP 76	PWRGD_50MS#	Inverted Power Good delayed 50 ms. 1K PU to + 3 V SB
GP 85	CPUFAN_TACH	Tach input from CPU fan connector; 4.7K PU to +3.3 V

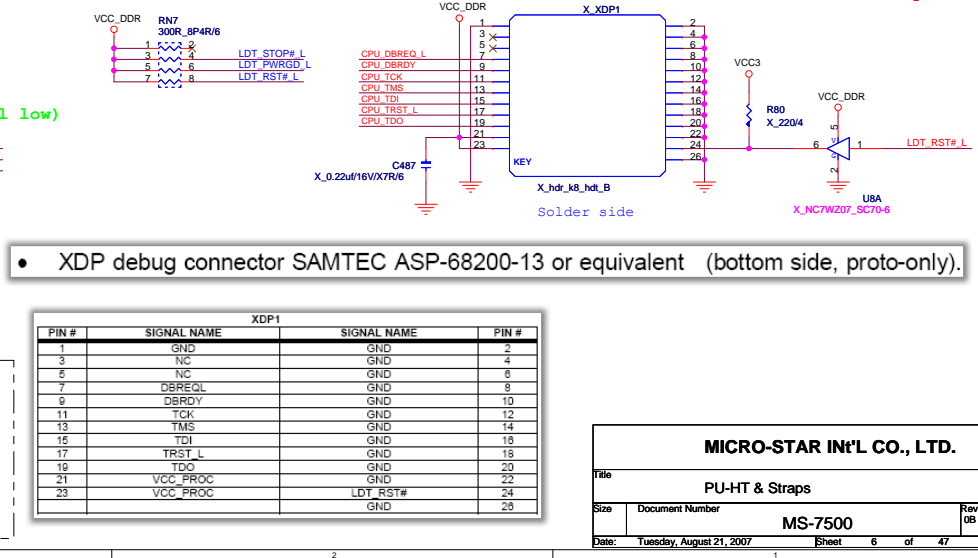
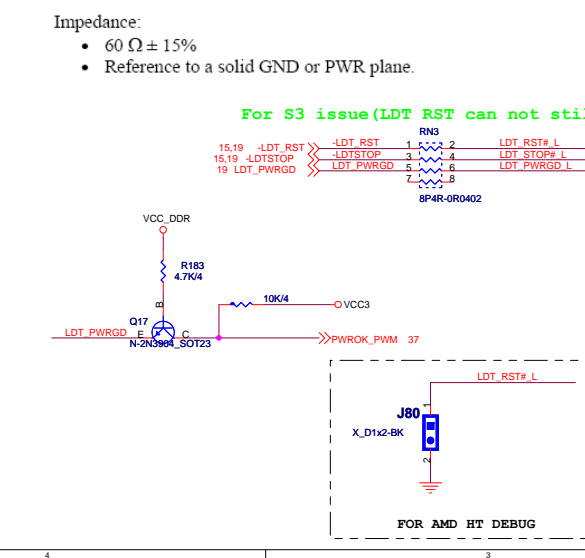
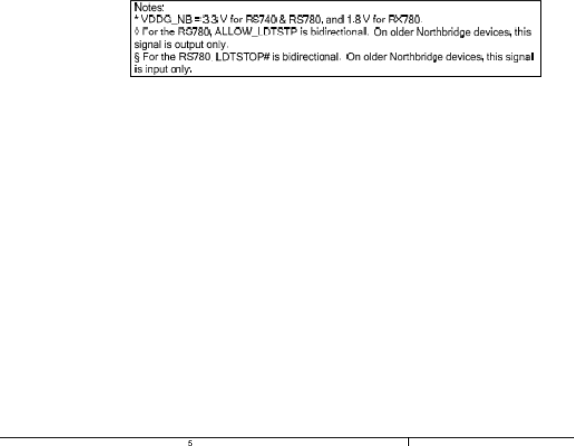
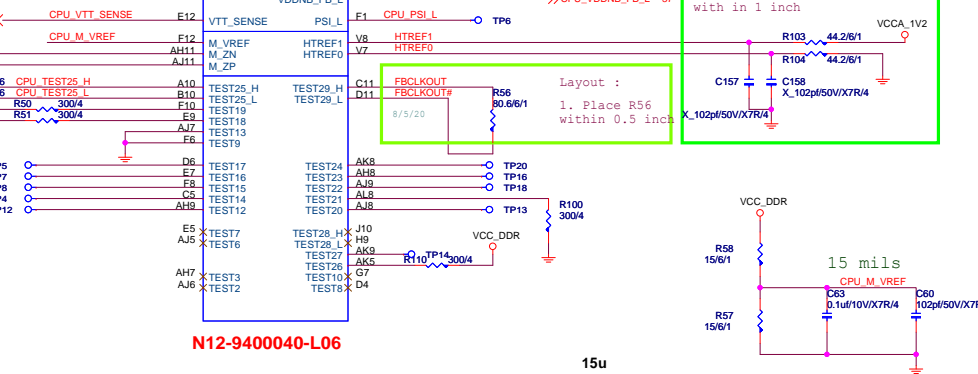
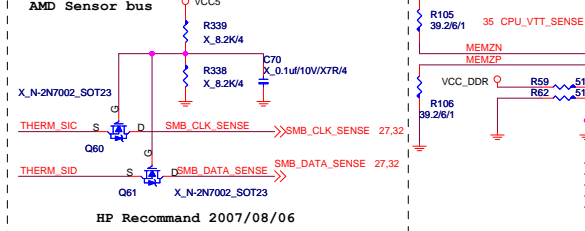
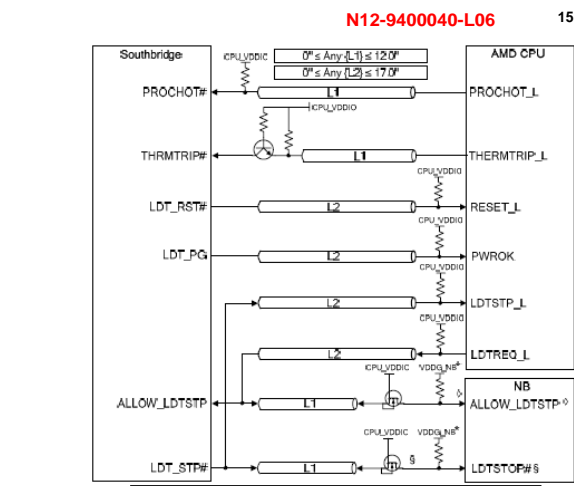
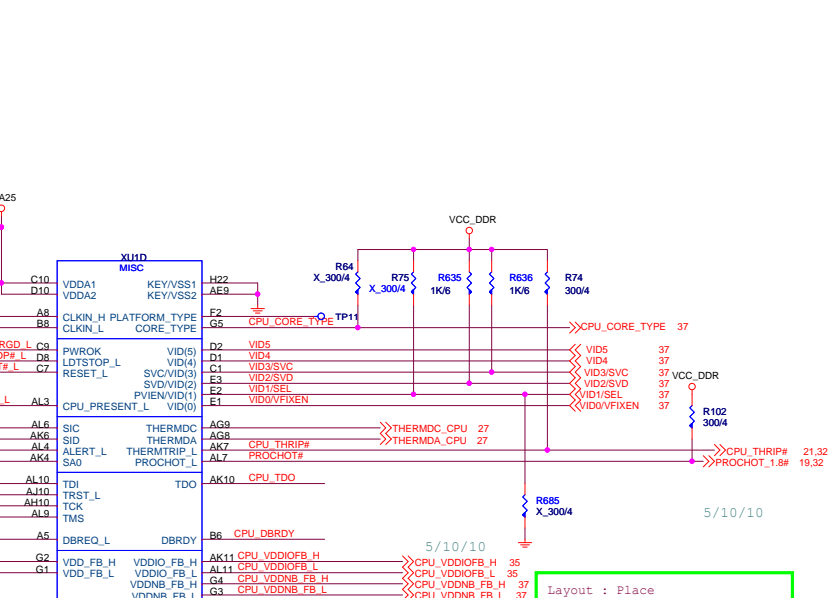
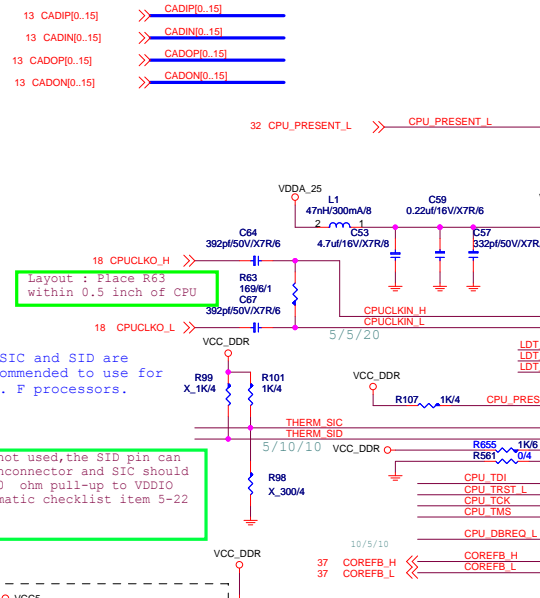
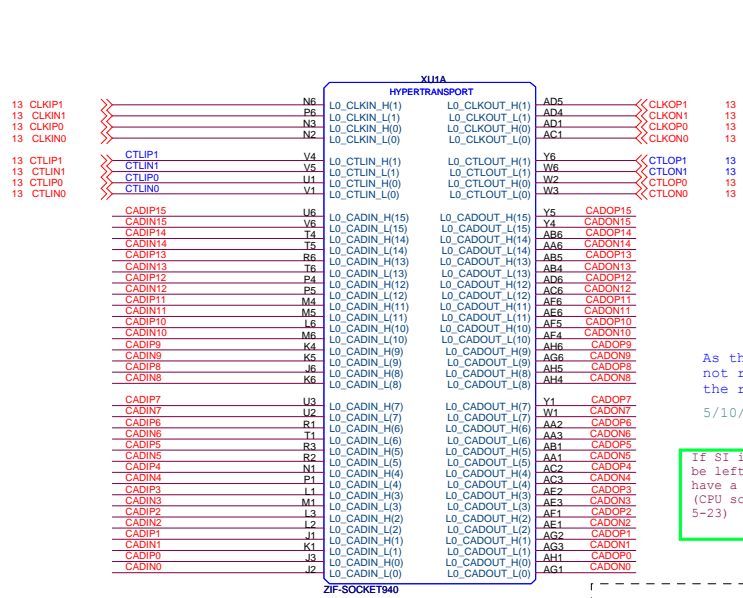
ATI SB700 GPIO Matrix

Pin Capabilities							Pin Defaults			BIOS Assignments				
			Strapping Function / Internal PU or PD	Input/ Output	Power Well	Voltage Tolerance	Default Signal Definition	Default Buffer Type	Default Output Level	Function	Input/ Output	Output Level	Motherboard Function	Implementation Notes
Pin	GPIO	Alternate Functions												
A27	GPIO 0			VO	Vcc3_3	5		I		GPIO 0	I		BRD_ID0	
A28	GPIO 4	ROM_CS#		VO	Vcc3_3	5		I		GPIO 1	I			
B28	GPIO 2	SPKR		VO	Vcc3_3	5		I		SPKR	O		SB000 SPKR OUT	
M4	GPIO 3	FANOUT0		VO	Vcc3_3	5		I		GPIO 3	I		PROCHOT2_SB	
B27	GPIO 4	SMARTVOLT/SATA_1S2#		VO	Vcc3_3	5		TRI-STATE		GPIO 4	I		BRD_REV0	
D23	GPIO 5	SHUTDOWN#		VO	Vcc3_3	5		TRI-STATE		GPIO 5	I		BRD_REV1	
B29	GPIO 6	OHM/SATA_1S1#		VO	Vcc3_3	5		TRI-STATE		GPIO 6	I		CHASSIS_ID0	
A23	GPIO 7	W0_PWRGD		VO	Vcc3_3	5		TRI-STATE		GPIO 7	I			
C28	GPIO 8	DDC1_SDA		VO	Vcc3_3	5		TRI-STATE		GPIO 8	I		CHASSIS_ID2	
D26	GPIO 9	DDC1_SCL		VO	Vcc3_3	5		TRI-STATE		GPIO 9	I		BRD_ID1	
C28	GPIO 10	SATA_ISO#		VO	Vcc3_3	3.3		TRI-STATE		GPIO 10	I		CHASSIS_ID1	
J6	GPIO 11	SPI_DO		VO	VccSUS3	3.3		TRI-STATE		SPI_DO	O		SPI DATA-OUT	
J3	GPIO 12	SPI_DI		VO	VccSUS3	3.3		TRI-STATE		SPI_DI	I		SPI DATA-IN	
C23	GPIO 13	LAN_RST#		OD	Vcc3_3	5		O						
G5	GPIO 14	ROM_RST#		VO	Vcc3_3	5		O		ROM_RST#	O		LPC ROM_RST#	
AD28	GPIO 15	IDE_D0		VO	Vcc3_3	5		TRI-STATE		IDE_D0	VO		IDE_D0	
AD26	GPIO 16	IDE_D1		VO	Vcc3_3	5		TRI-STATE		IDE_D1	VO		IDE_D1	
AE29	GPIO 17	IDE_D2		VO	Vcc3_3	5		TRI-STATE		IDE_D2	VO		IDE_D2	
AF27	GPIO 18	IDE_D3		VO	Vcc3_3	5		TRI-STATE		IDE_D3	VO		IDE_D3	
AG29	GPIO 19	IDE_D4		VO	Vcc3_3	5		TRI-STATE		IDE_D4	VO		IDE_D4	
AH28	GPIO 20	IDE_D5		VO	Vcc3_3	5		TRI-STATE		IDE_D5	VO		IDE_D5	
AJ28	GPIO 21	IDE_D6		VO	Vcc3_3	5		TRI-STATE		IDE_D6	VO		IDE_D6	
AJ27	GPIO 22	IDE_D7		VO	Vcc3_3	5		TRI-STATE		IDE_D7	VO		IDE_D7	
AH27	GPIO 23	IDE_D8		VO	Vcc3_3	5		TRI-STATE		IDE_D8	VO		IDE_D8	
AG27	GPIO 24	IDE_D9		VO	Vcc3_3	5		TRI-STATE		IDE_D9	VO		IDE_D9	
AG28	GPIO 25	IDE_D10		VO	Vcc3_3	5		TRI-STATE		IDE_D10	VO		IDE_D10	
AF28	GPIO 26	IDE_D11		VO	Vcc3_3	5		TRI-STATE		IDE_D11	VO		IDE_D11	
AG29	GPIO 27	IDE_D12		VO	Vcc3_3	5		TRI-STATE		IDE_D12	VO		IDE_D12	
AE28	GPIO 28	IDE_D13		VO	Vcc3_3	5		TRI-STATE		IDE_D13	VO		IDE_D13	
AD25	GPIO 29	IDE_D14		VO	Vcc3_3	5		TRI-STATE		IDE_D14	VO		IDE_D14	
AD29	GPIO 30	IDE_D15		VO	Vcc3_3	5		TRI-STATE		IDE_D15	VO		IDE_D15	
G2	GPIO 31	SPI_HOLD#		VO	VccSUS3	3.3		TRI-STATE		SPI_HOLD#	O		SPI_HOLD#	
G6	GPIO 32	SPI_CS#		VO	VccSUS3	3.3		TRI-STATE		SPI_CS#	O		SPI CHIP SELECT#	
AD3	GPIO 33	INT#		VO	Vcc3_3	5		TRI-STATE		INT#	I		PCI INT#	To PCI slots J21 & J22.
AF1	GPIO 34	INT#		VO	Vcc3_3	5		TRI-STATE		INT#	I		PCI INT#	To PCI slots J21 & J22.
AF4	GPIO35	INT#		VO	Vcc3_3	5		TRI-STATE		INT#	I		PCI INT#	To PCI slots J21 & J22.
AF3	GPIO36	INT#		VO	Vcc3_3	5		TRI-STATE		INT#	I		PCI INT#	To PCI slots J21 & J22.
B24	GPIO37	DRSLP_OD#	Open drain. Requires external pullup to Vcc3_3	VO	Vcc3_3	5		TRI-STATE						
L1	GPIO38	AC_BITCLK		VO	Vcc3_3	5		I						
L2	GPIO39	AC_SDOUT	STRAP: 10k pullup to Vcc3_3. 10k pullup to Vcc3_3. 10k pullup to Vcc3_3.	VO	Vcc3_3	5		O						
M2	GPIO40	CLK_REG2/SATA_1S5		VO	Vcc3_3	5		I		GPIO 40	I		PRT_DET#	
T1	GPIO41	PCICLK#		VO	Vcc3_3	5		O						
L4	GPIO42	AZ_SDIN0		VO	VccSUS3	3.3		I						
J2	GPIO43	AZ_SDIN1		VO	VccSUS3	3.3		I						
J4	GPIO44	AZ_SDIN2		VO	VccSUS3	3.3		I						
L5	GPIO45	AC_RST#		VO	VccSUS3	3.3		O		GPIO 45	O			
K2	GPIO46	AZ_SDIN3		VO	Vcc3_3	5		I		ACC_SDIN3	I		AZALIA AUDIO IN	
G3	GPIO47	SPI_CLK		VO	VccSUS3	3.3		O		SPI_CLK	O		SPI CLOCK	
T3	GPIO 48	FANOUT1		VO	Vcc3_3	3.3		TRI-STATE		GPIO 48	I		COMM_B_DET#	
V4	GPIO 49	FANOUT2		VO	Vcc3_3	3.3		TRI-STATE		GPIO 49	I		FRONT_AUD_DET#	
N3	GPIO 50	FANIN0		VO	Vcc3_3	3.3		TRI-STATE		GPIO 50	I		FRONT_USB_DET#	
P2	GPIO 51	FANIN1		VO	Vcc3_3	3.3		TRI-STATE		GPIO 51	I		FLASH_SEC_OVERRIDE	
W4	GPIO 52	FANIN2		VO	Vcc3_3	3.3		TRI-STATE		GPIO 52	I		PASSWORD_ENABLE	
V5	GPIO 53	VIN0		VO	Vcc3_3	3.3		TRI-STATE		GPIO 53	I		BOOT_BLOCK_ENAB	
L7	GPIO 54	VIN1		VO	Vcc3_3	3.3		TRI-STATE		GPIO 54	I		BOOT_BLOCK_RECOVERY#	
M8	GPIO 55	VIN2		VO	Vcc3_3	3.3		TRI-STATE		GPIO 55	I		BRD_ID2	
V6	GPIO 56	VIN3		VO	Vcc3_3	3.3		TRI-STATE						
M9	GPIO 57	VIN4		VO	Vcc3_3	3.3		TRI-STATE						
P4	GPIO 58	VIN5		VO	Vcc3_3	3.3		TRI-STATE						
M7	GPIO 59	VIN6		VO	Vcc3_3	3.3		TRI-STATE						
V7	GPIO 60	VIN7		VO	Vcc3_3	3.3		TRI-STATE						
P7	GPIO 61	TEMPIN0		VO	Vcc3_3	3.3		TRI-STATE						
P8	GPIO 62	TEMPIN1		VO	Vcc3_3	3.3		TRI-STATE						
T8	GPIO 63	TEMPIN2		VO	Vcc3_3	3.3		TRI-STATE						
T7	GPIO 64	TEMPIN3/TALERT#		VO	Vcc3_3	3.3		TRI-STATE						
W22	GPIO 65	BMREQ#/REQ0#		VO	Vcc3_3	3.3		TRI-STATE		BMREQ#	I			
A4	GPIO 66	LLB#		VO	VccSUS3	3.3		TRI-STATE						
AC12	GPIO 67	SATA_ACT#		VO	Vcc3_3	3.3		TRI-STATE		SATA_ACT	O		SATA_LED	
AH28	GPIO 68	LDRQ1#/GNT5#		VO	Vcc3_3	5		TRI-STATE		LDRQ1#	I			
F5	GPIO 69	RTC_IRQ#		VO	3V/BAT	3.3		O						
AH8	GPIO 70	REQ0#		VO	Vcc3_3	5		TRI-STATE						
AH5	GPIO 71	REQ4#		VO	Vcc3_3	5		TRI-STATE						
AB12	GPIO 72	GNT3#		VO	Vcc3_3	5		O						
AG4	GPIO 73	GNT4#		VO	Vcc3_3	5		O						

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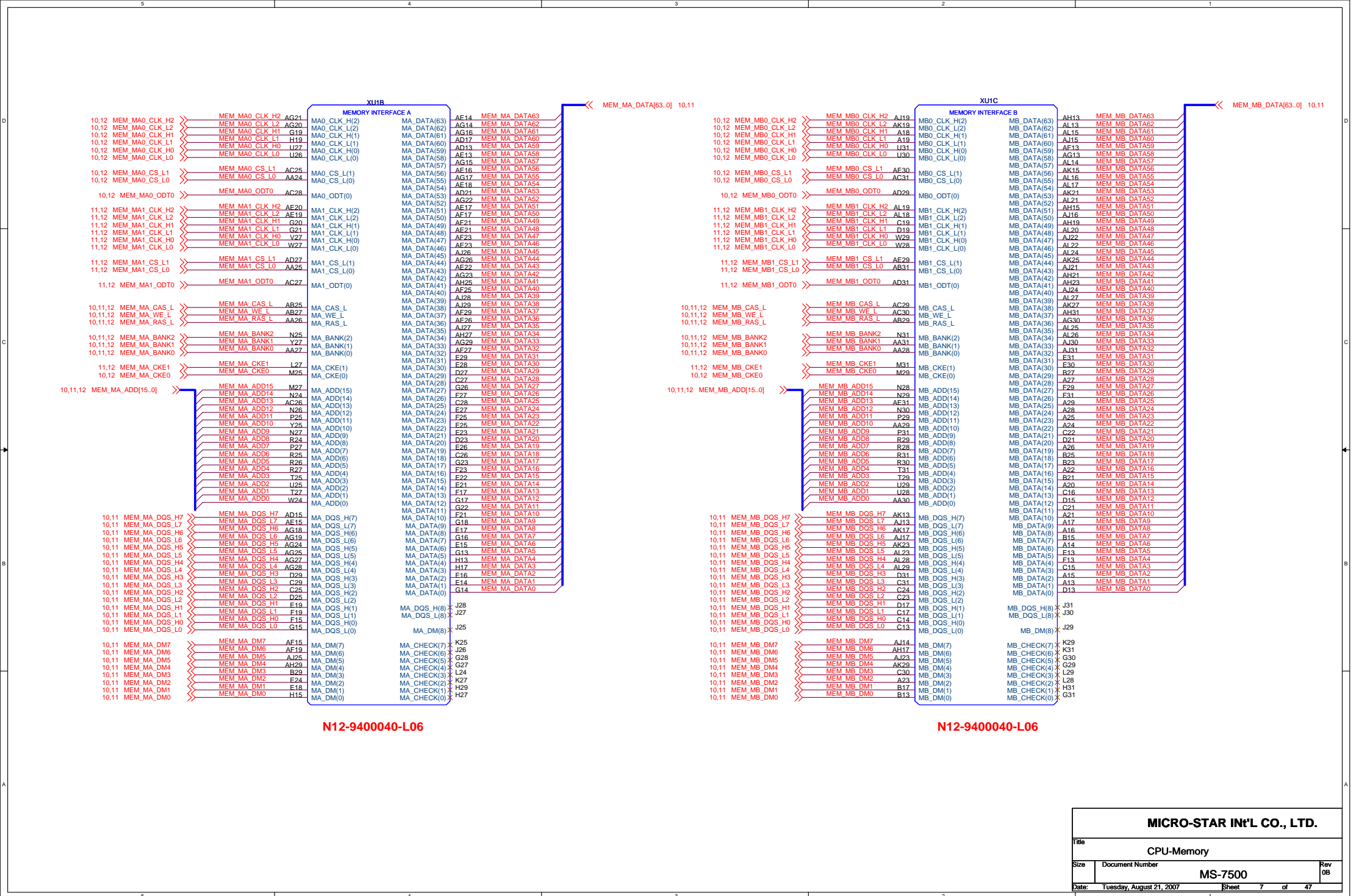
Title			GPIO Table
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• XDP debug connector SAMTEC ASP-68200-13 or equivalent (bottom side, proto-only).

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	GND	GND	2
3	NC	GND	4
5	NC	GND	6
7	DBREQ	GND	8
9	DBREQ	GND	10
11	GND	GND	12
13	TMS	GND	14
15	TDI	GND	16
17	TRST_L	GND	18
19	TDO	GND	20
21	VCC_PROC	GND	22
23	VCC_PROC	GND	24



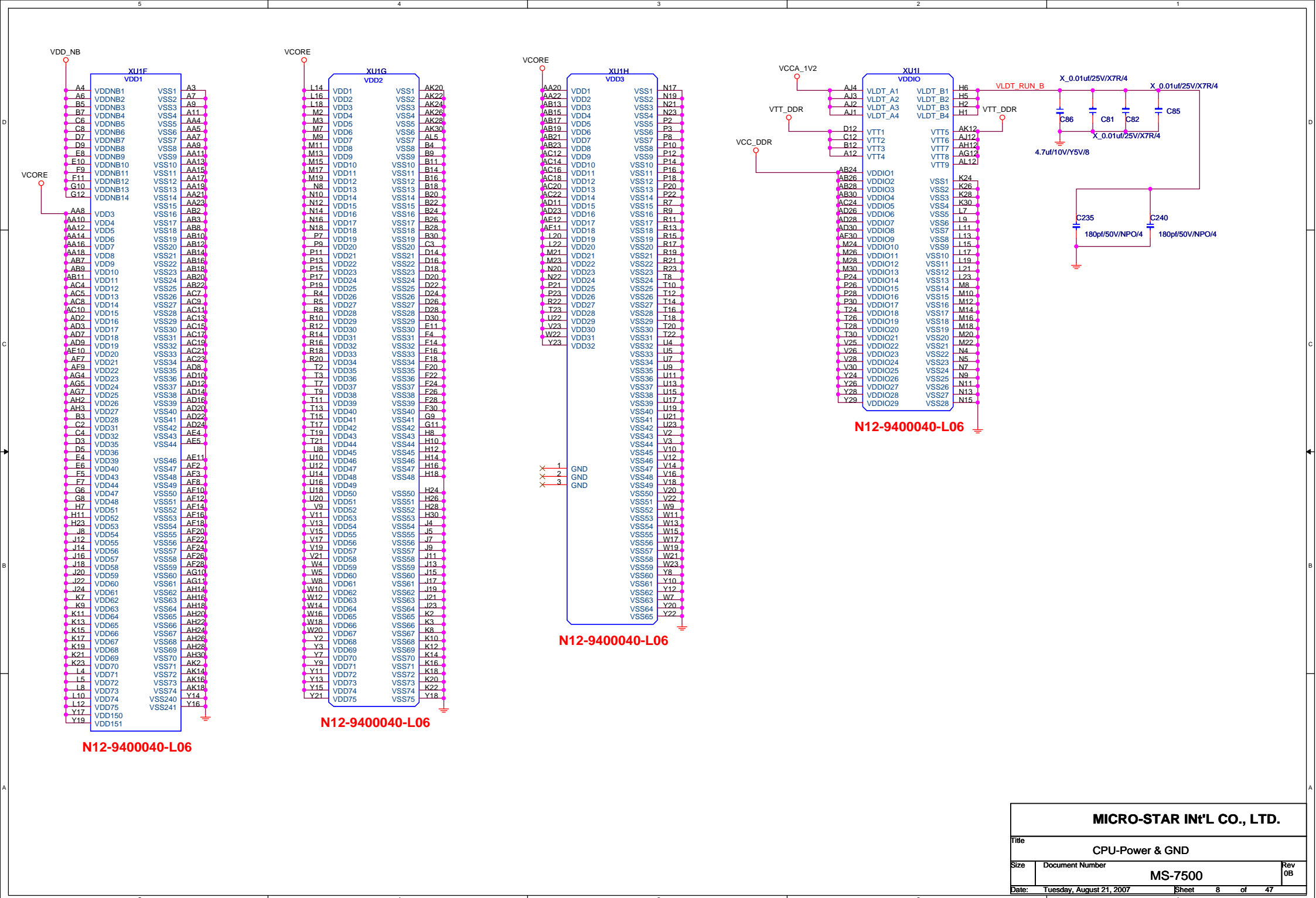
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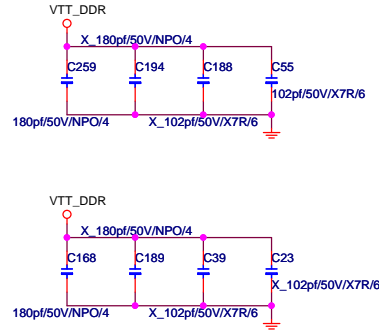


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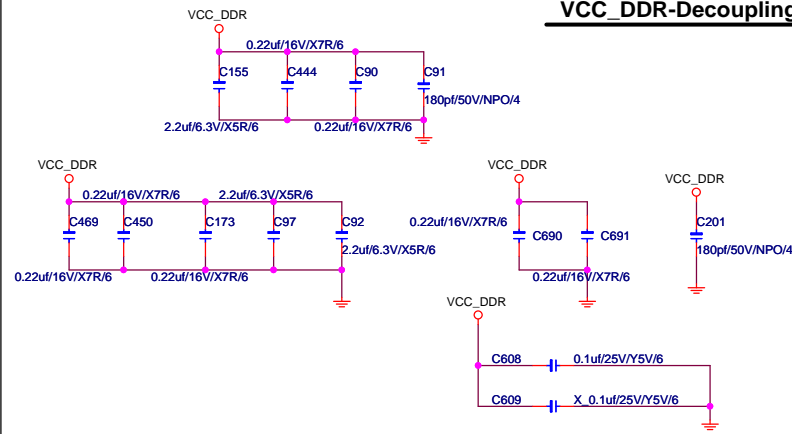
Title			CPU-Power & GND
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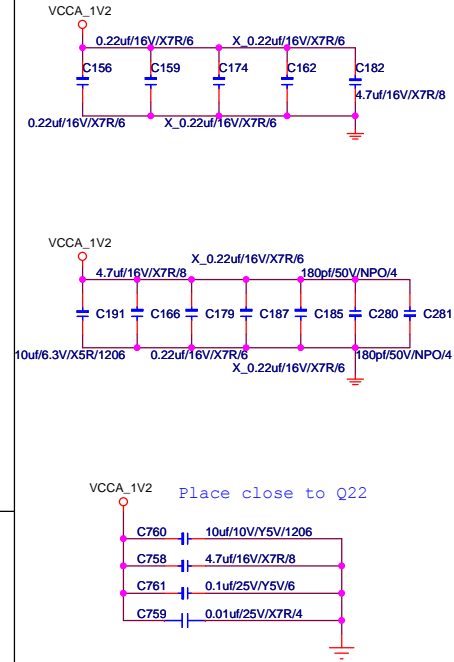
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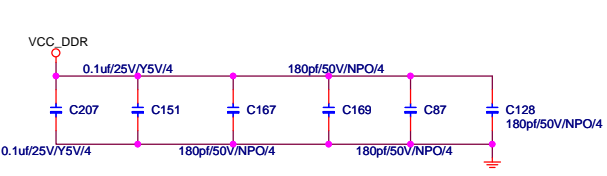
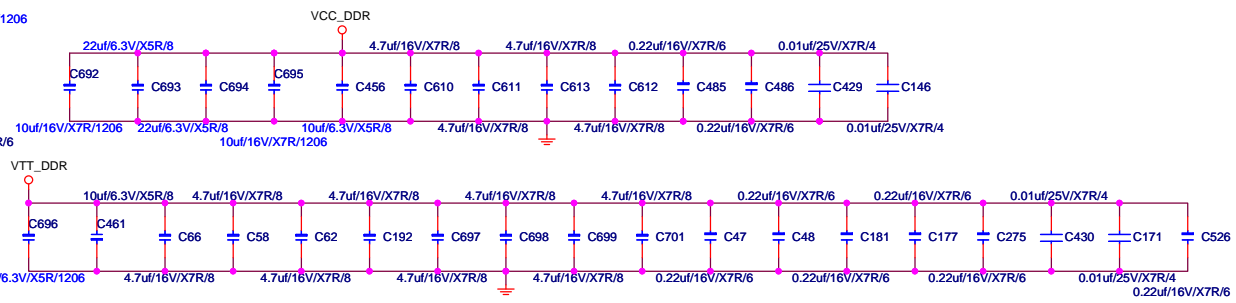
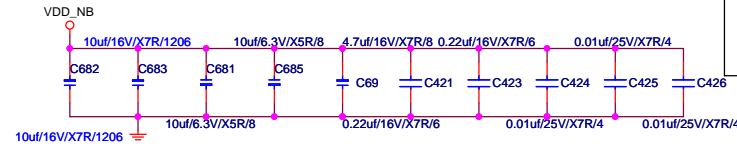
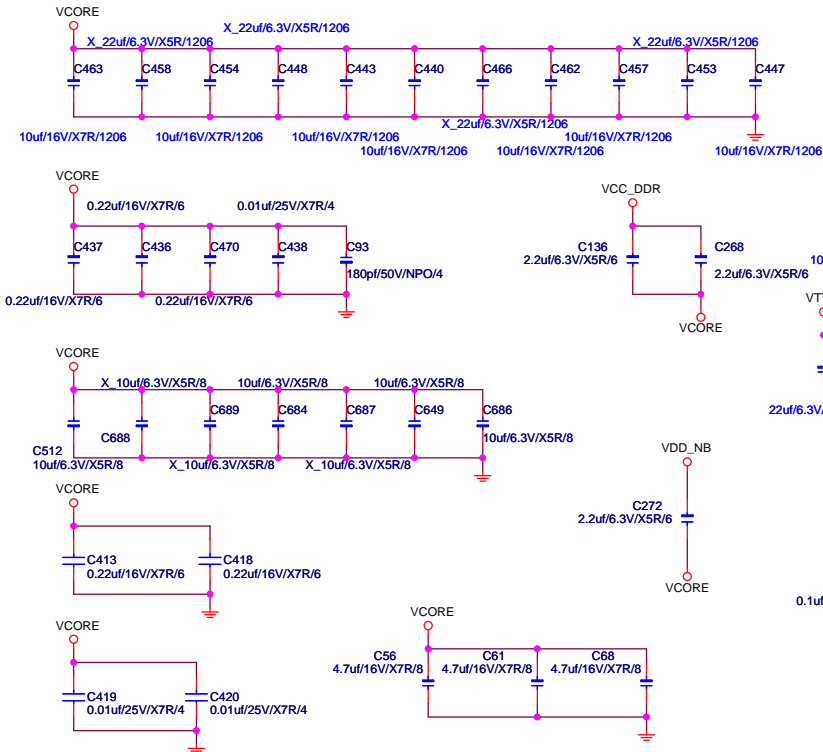
### VCC\_DDR-Decoupling



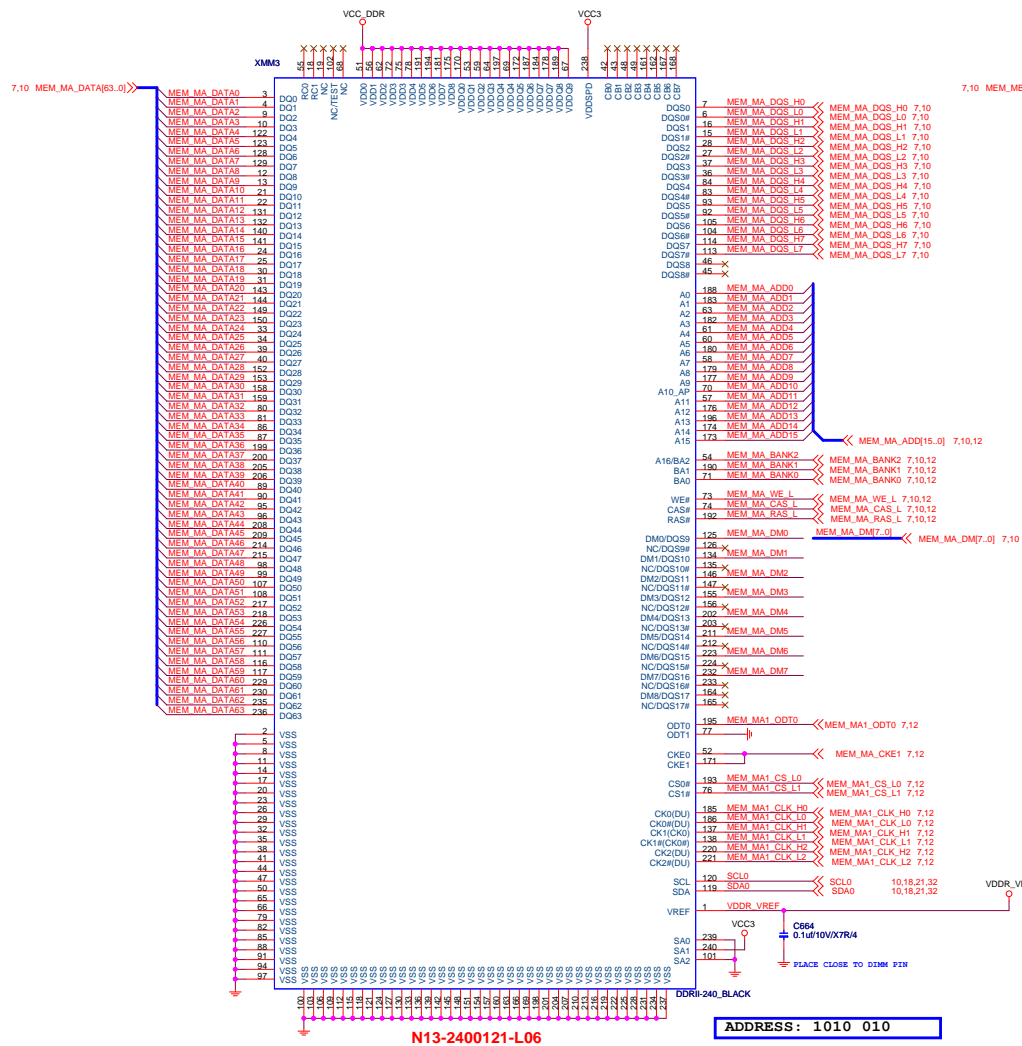
### VCCA\_1V2-Decoupling



### VCORE-Decoupling

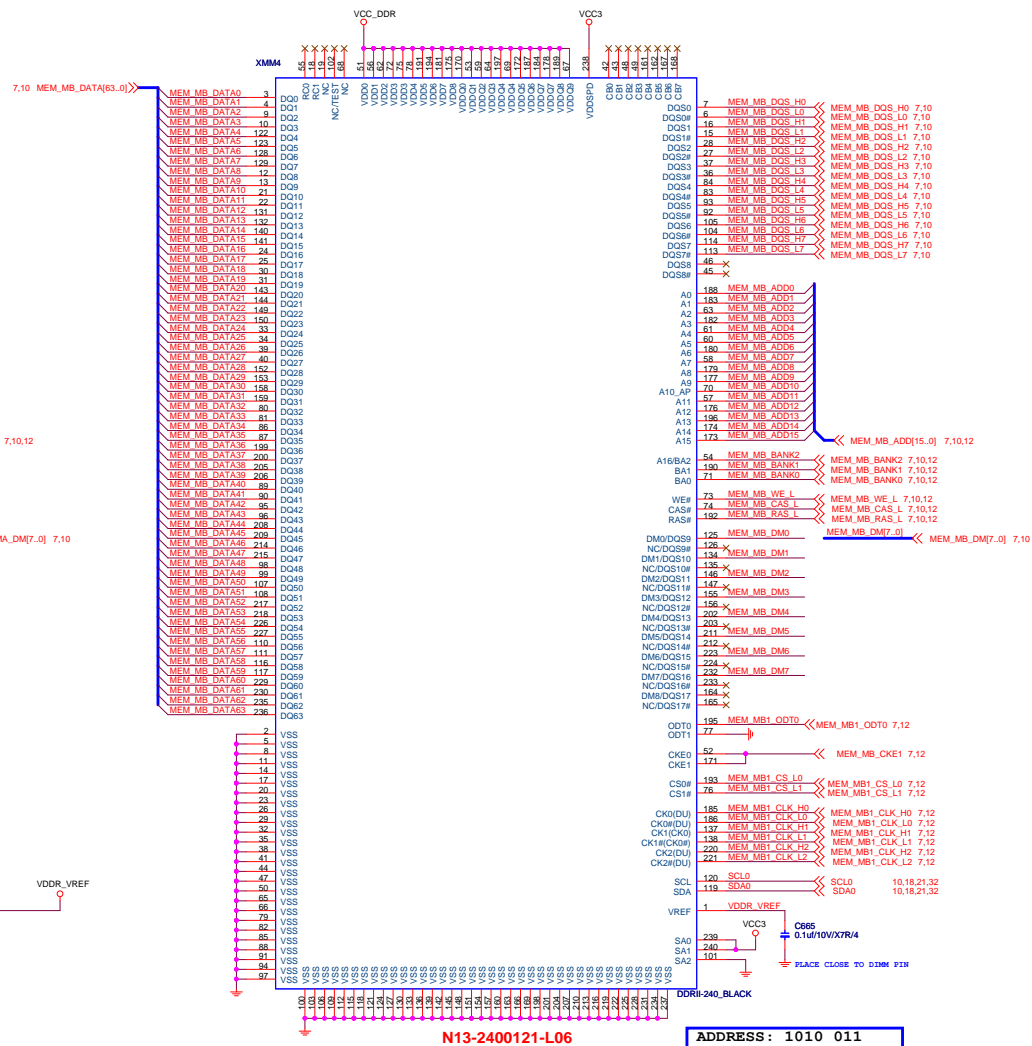






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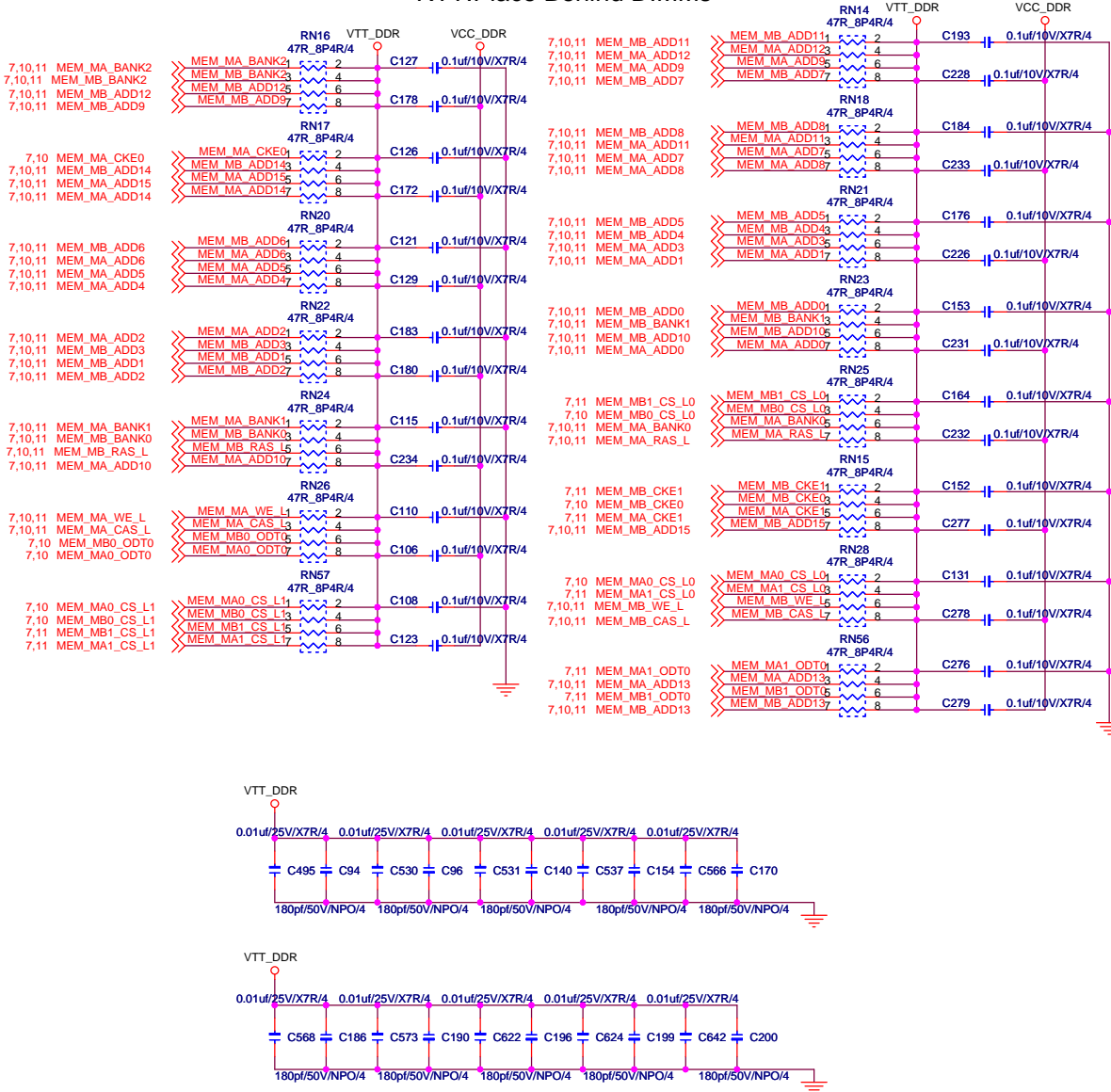
BLACK COLOR



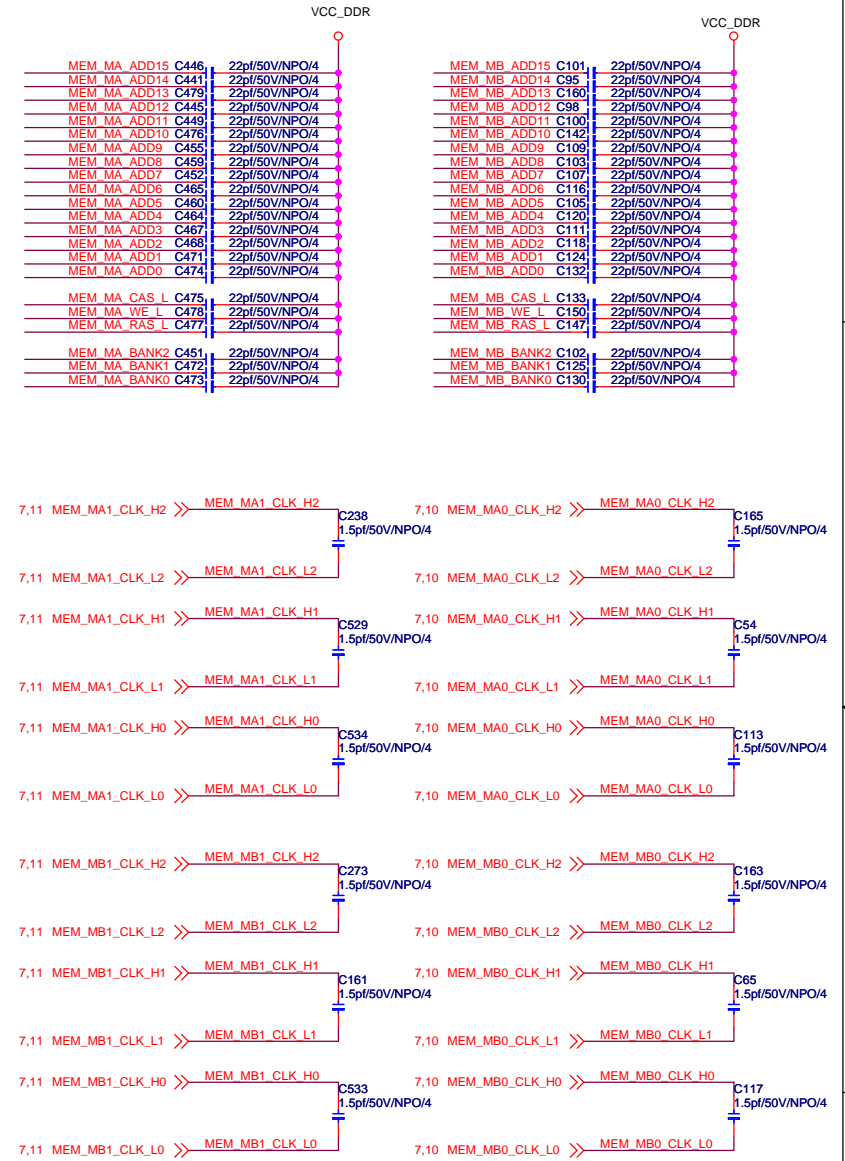
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BLACK COLOR

## RTT:Place Behind DIMMs



## Place Between Processor and DIMMs



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6 CADOP[0..15] &gt;&gt; CADOP[0..15]

6 CADON[0..15] &gt;&gt; CADON[0..15]

20 / 5 / 5 / 5 / 20

CADOP0 Y25 HT\_RXCAD0P  
CADON0 Y24 HT\_RXCAD0N  
CADOP1 V22 HT\_RXCAD1P  
CADON1 V23 HT\_RXCAD1N  
CADOP2 V25 HT\_RXCAD2P  
CADON2 V24 HT\_RXCAD2N  
CADOP3 U24 HT\_RXCAD3P  
CADON3 U25 HT\_RXCAD3N  
CADOP4 T25 HT\_RXCAD4P  
CADON4 T24 HT\_RXCAD4N  
CADOP5 P22 HT\_RXCAD5P  
CADON5 P23 HT\_RXCAD5N  
CADOP6 P25 HT\_RXCAD6P  
CADON6 P24 HT\_RXCAD6N  
CADOP7 N24 HT\_RXCAD7P  
CADON7 N25 HT\_RXCAD7N

CADOP8 AC24 HT\_RXCAD8P  
CADON8 AC25 HT\_RXCAD8N  
CADOP9 AB24 HT\_RXCAD9P  
CADON9 AB25 HT\_RXCAD9N  
CADOP10 AA24 HT\_RXCAD10P  
CADON10 AA25 HT\_RXCAD10N  
CADOP11 Y22 HT\_RXCAD11P  
CADON11 Y23 HT\_RXCAD11N  
CADOP12 W21 HT\_RXCAD12P  
CADON12 W20 HT\_RXCAD12N  
CADOP13 V21 HT\_RXCAD13P  
CADON13 V20 HT\_RXCAD13N  
CADOP14 U20 HT\_RXCAD14P  
CADON14 U21 HT\_RXCAD14N  
CADOP15 U19 HT\_RXCAD15P  
CADON15 U18 HT\_RXCAD15N

6 CLKOP0 >> CLKOP0 T22 HT\_RXCLK0P  
6 CLKON0 >> CLKON0 T23 HT\_RXCLK0N  
6 CLKOP1 >> CLKOP1 AB23 HT\_RXCLK1P  
6 CLKON1 >> CLKON1 AA22 HT\_RXCLK1N

6 CTLOP0 >> CTLOP0 M22 HT\_RXCTL0P  
6 CTLOP1 >> CTLOP1 M23 HT\_RXCTL0N  
6 CTLOP2 >> CTLOP2 R21 HT\_RXCTL1P  
6 CTLOP3 >> CTLOP3 R20 HT\_RXCTL1N

301/4/1 R34 HT\_RXCALP C23 HT\_RXCALP  
HT\_RXCALN A24 HT\_RXCALN

5 / 10

AMD-215NDA78KA11FG-A11-RH

PART 1 OF 6

HYPER TRANSPORT CPU  
I/F

HT\_TXCAD0P D24 CADIP0  
HT\_TXCAD0N D25 CADIN0  
HT\_TXCAD1P E24 CADIP1  
HT\_TXCAD1N E25 CADIN1  
HT\_TXCAD2P F24 CADIP2  
HT\_TXCAD2N F25 CADIN2  
HT\_TXCAD3P F23 CADIP3  
HT\_TXCAD3N F22 CADIN3  
HT\_TXCAD4P H23 CADIP4  
HT\_TXCAD4N H22 CADIN4  
HT\_TXCAD5P J25 CADIP5  
HT\_TXCAD5N J24 CADIN5  
HT\_TXCAD6P K24 CADIP6  
HT\_TXCAD6N K25 CADIN6  
HT\_TXCAD7P K23 CADIP7  
HT\_TXCAD7N K22 CADIN7

HT\_TXCAD8P F21 CADIP8  
HT\_TXCAD8N G21 CADIN8  
HT\_TXCAD9P G20 CADIP9  
HT\_TXCAD9N H21 CADIN9  
HT\_TXCAD10P J20 CADIP10  
HT\_TXCAD10N J21 CADIN10  
HT\_TXCAD11P J18 CADIP11  
HT\_TXCAD11N K17 CADIN11  
HT\_TXCAD12P L19 CADIP12  
HT\_TXCAD12N L18 CADIN12  
HT\_TXCAD13P M19 CADIP13  
HT\_TXCAD13N L18 CADIN13  
HT\_TXCAD14P M21 CADIP14  
HT\_TXCAD14N P21 CADIN14  
HT\_TXCAD15P P18 CADIP15  
HT\_TXCAD15N M18 CADIN15

H24 CLKIP0 >> CLKIP0 6  
H25 CLKIN0 >> CLKIN0 6  
L21 CLKIP1 >> CLKIP1 6  
L20 CLKIN1 >> CLKIN1 6

M24 CTLIPO >> CTLIPO 6  
M25 CTLIN0 >> CTLIN0 6  
P19 CTLIP1 >> CTLIP1 6  
P18 CTLIN1 >> CTLIN1 6

B24 HT\_TXCALP R36 301/4/1  
B25 HT\_TXCALN

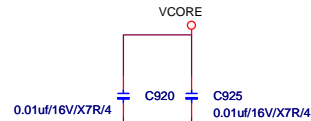
5 / 10

CADIP[0..15] &gt;&gt; CADIP[0..15] 6

CADIN[0..15] &gt;&gt; CADIN[0..15] 6

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



Adding some 0.01 $\mu$ F stitching capacitors for crossing a split when these signals change different reference layer.

For 07/09/07

MICRO-STAR IN'L CO., LTD.

Title

RS780/RX780-HT LINK I/F

Size

Document Number

MS-7500

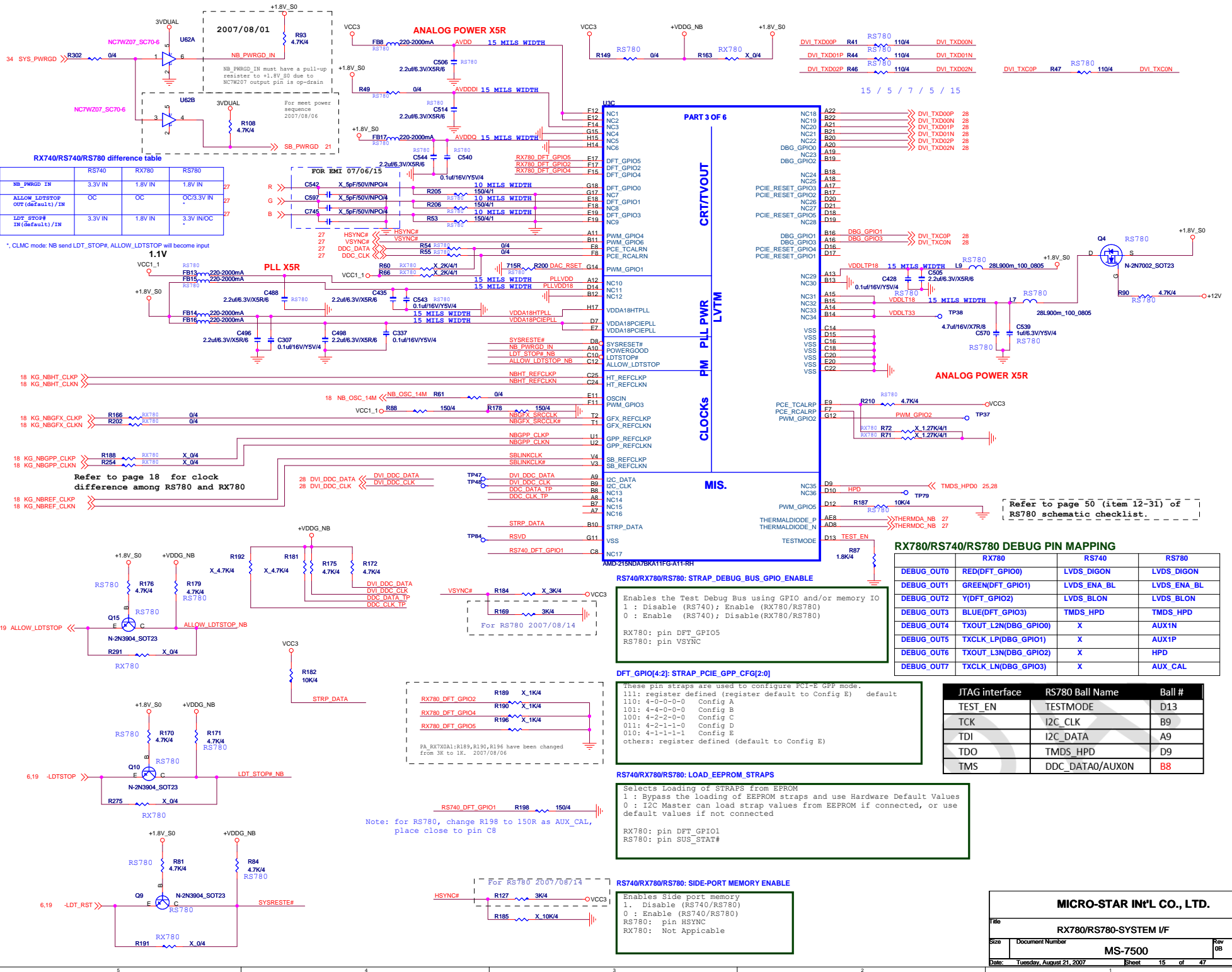
Rev

0B

Date: Tuesday, August 21, 2007

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**RX740/RX780/R5780 difference table**

	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP_OUT (default) / IN	OC	OC	OC/3.3V IN
LDT_STOP# IN (default) / IN	3.3V IN	1.8V IN	3.3V IN/OC

\*, CLMC mode: NB send LDT\_STOP#, ALLOW\_LDTSTOP# will become input

**RX780/RX740/R5780 DEBUG PIN MAPPING**

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLOK	LVDS_BLOK
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

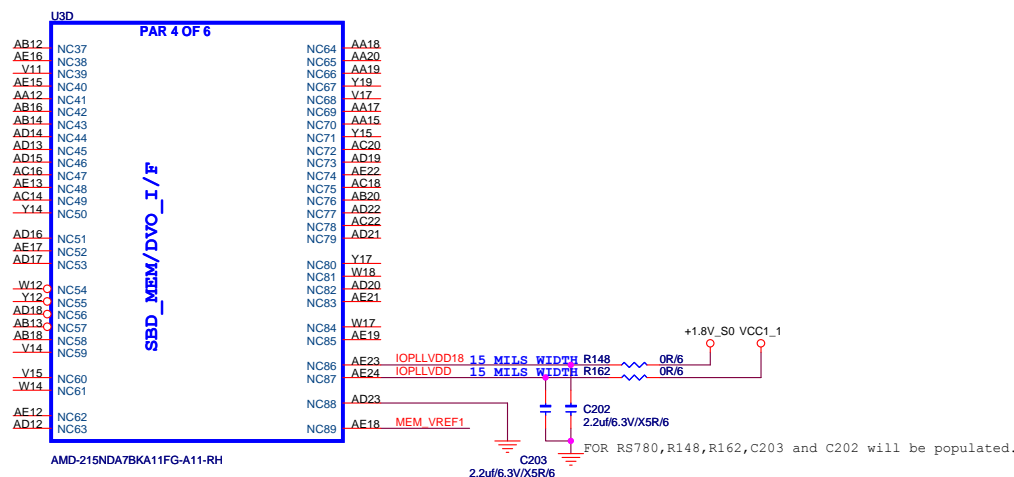
**JTAG interface**

TEST_EN	TESTMODE	D13
TCK	I2C_CLK	B9
TDI	I2C_DATA	A9
TDO	TMDS_HPD	D9
TMS	DDC_DATA0/AUX0N	B8

**MICRO-STAR INT'L CO., LTD.**

RX780/RX780-SYSTEM I/F		
Size	Document Number	Rev
	MS-7500	03
Date:	Tuesday, August 21, 2007	Sheet 15 of 47



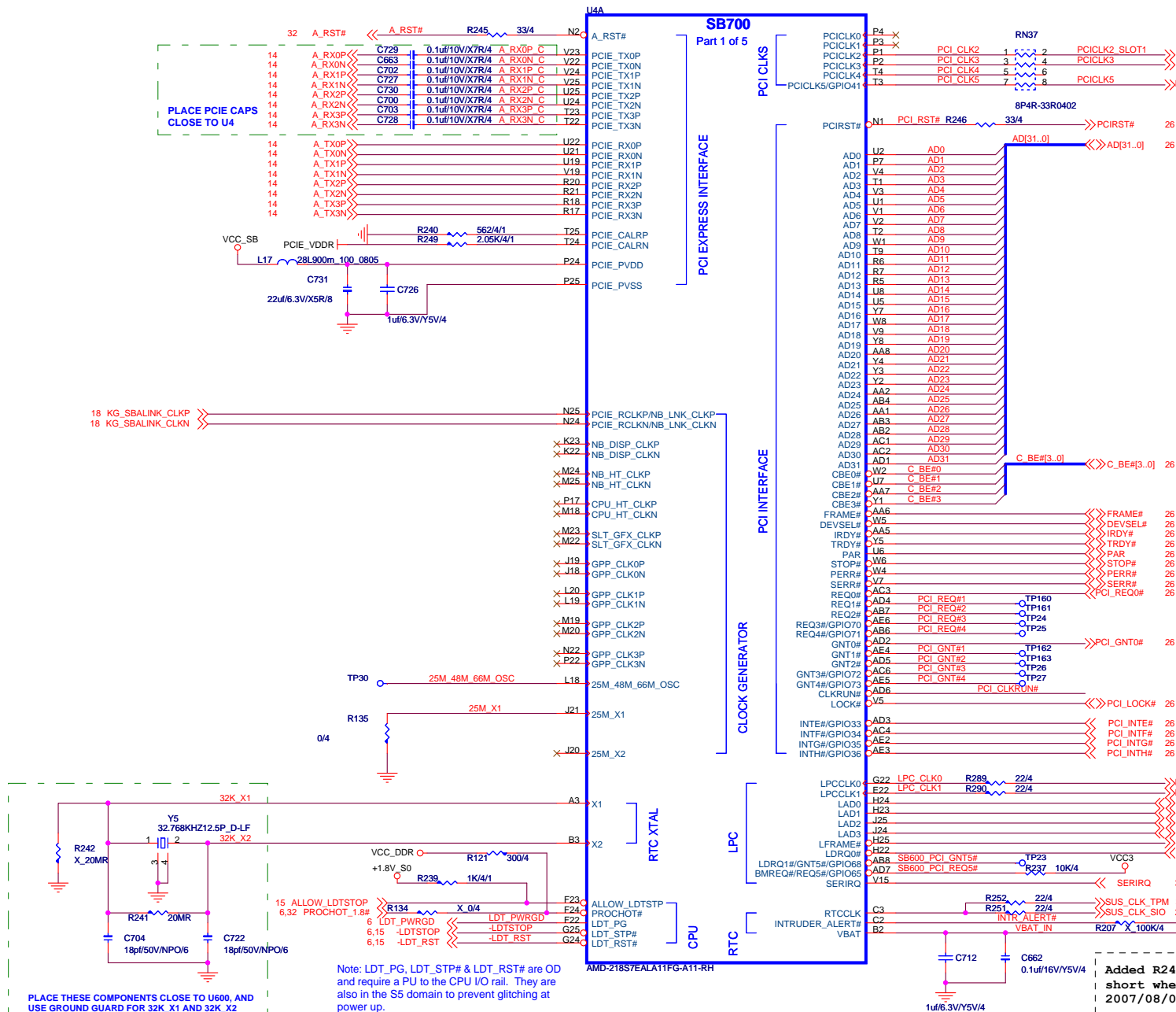
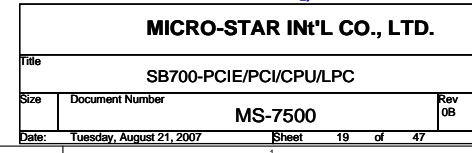
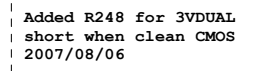
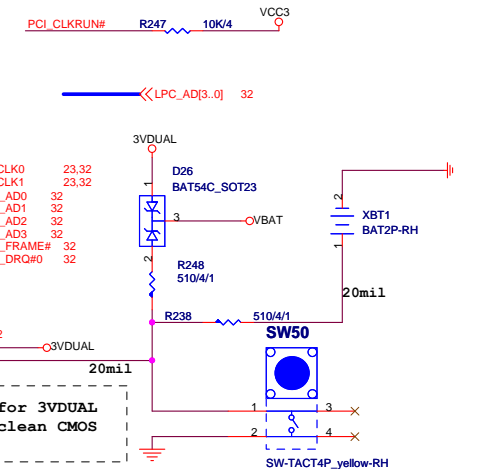
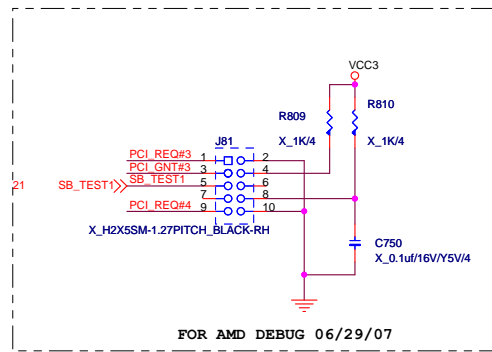
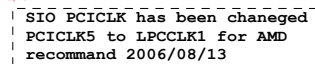


**Note:** If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD\_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18\_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM\_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT\_GPIO0 is **not** connected to the GND.





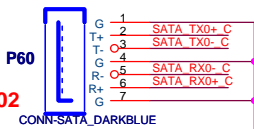


Note: LDT\_PG, LDT\_STP# & LDT\_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

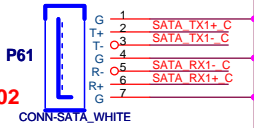


4 Ss	3 Ps
1 Pm	2 Sm

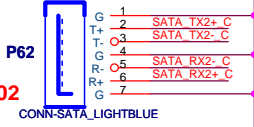
N5N-07M0561-F02



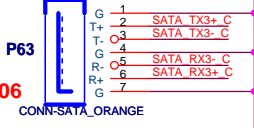
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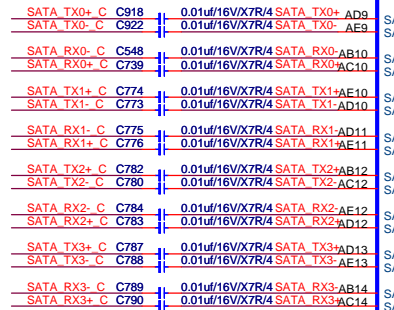
N5N-07M0581-F02



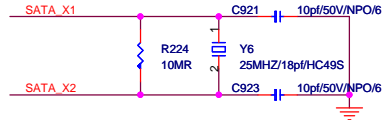
N5N-07M0431-H06



PLACE SATA AC COUPLING CAPS CLOSE TO SB700



R219 IS 1K 1% FOR XTAL, 4.99K 1% FOR INTERNAL CLK



SB700 Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR

AMD-218S7EALA11FGA11-RH

SB700 internal prll-up to 3.3V\_S0 2007/08/13

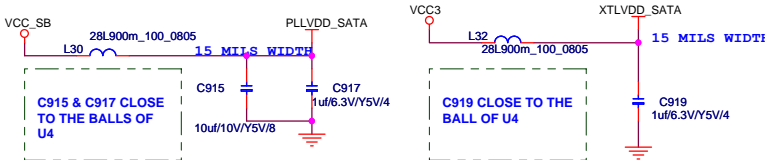
Figure 29: Layout Guidelines the Serial ATA Signals

Trace spacing:

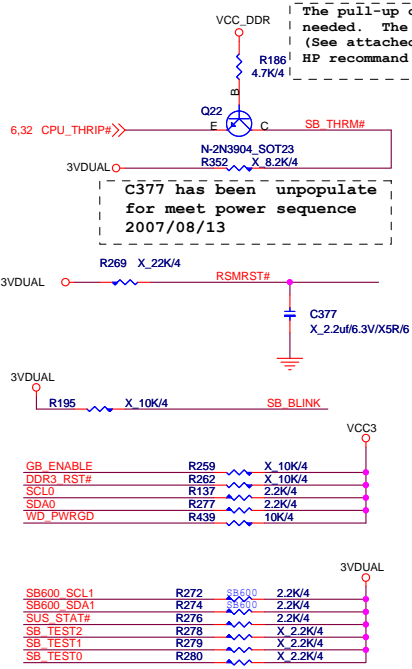
- ASIC breakout (first 0.5")  $\geq 1:1$
- After the breakout region  $\geq 5:1$  on both sides of pair.

Impedance:

- 100  $\Omega \pm 15\%$  differential.
- Reference to a solid GND (not PWR) plane.



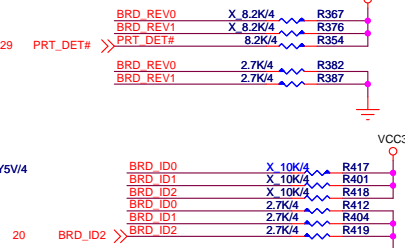
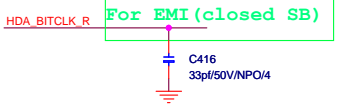
MICRO-STAR INT'L CO., LTD.			
Title SB700-SATA/IDE/HWM/SPI			
Size	Document Number	MS-7500	Rev 0B
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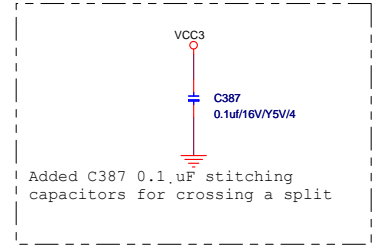
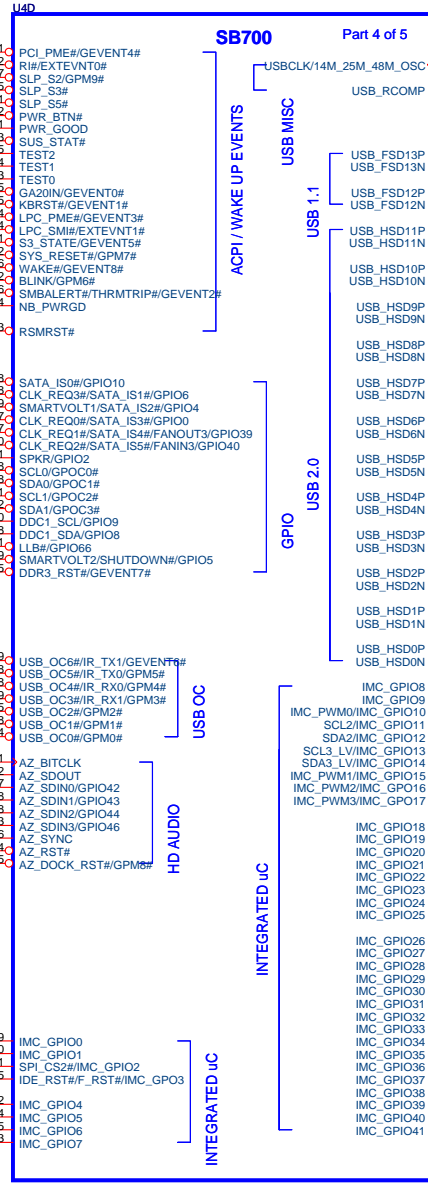
The pull-up on the SB700 side of the transistor is not needed. The SB700 has a default internal 10k pull-up. (See attached pic for reference) MSI can NI R352 for HP recommend 2007/08/19

Modify PRT\_DET# circuit 2006/08/06

BOARD ID[2:0]	PHASE
001	USDT
010	CMT
011	SFF



BOARD_REV[1:0]	PHASE
00	All Proto
01	All SI
10	PV1
11	PV2
00	MVB
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN



- Trace spacing:
- ASIC breakout (first 0.5")  $\geq 1:1$
  - After the breakout region  $\geq 1$  on both sides of pair.
  - Serpentine spacing  $\geq 4:1$  on both sides of pair.
  - $\geq 5:1$  from reference plane anti-etch (copper void) or edges.
  - $\geq 0.5"$  from clock chips, oscillators, crystals, core logic or CPU devices.
- Impedance:
- $90 \Omega \pm 15\%$  differential
  - Reference to a solid GND (not PWR) plane.

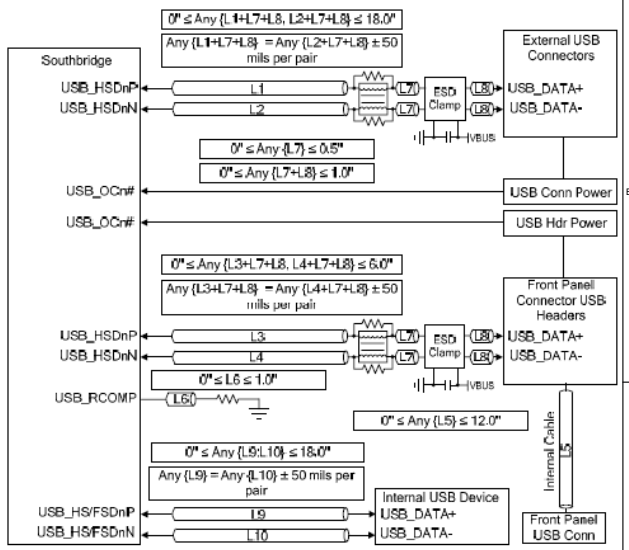
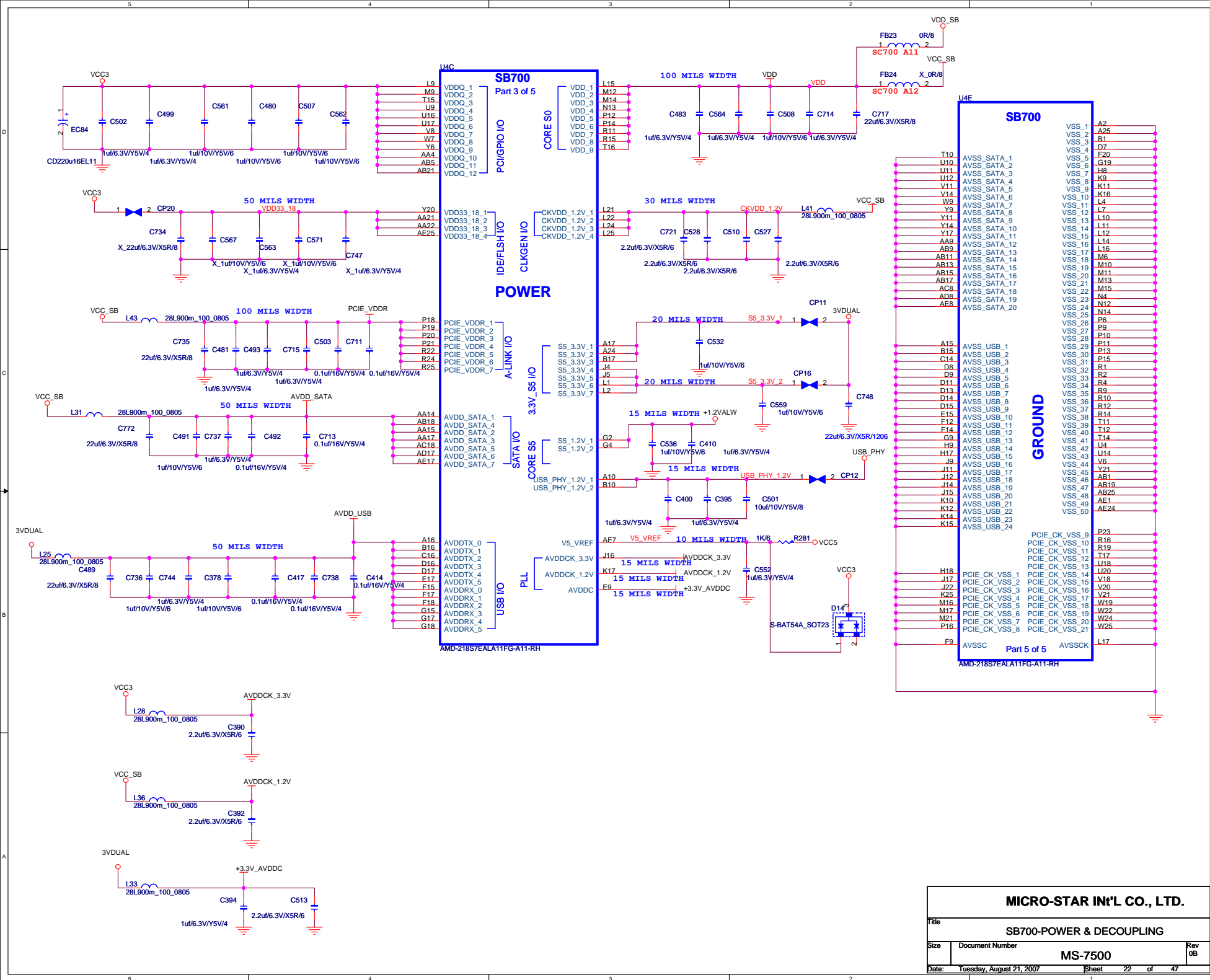


Figure 26 Layout Guidelines for the Universal Serial Bus Signals



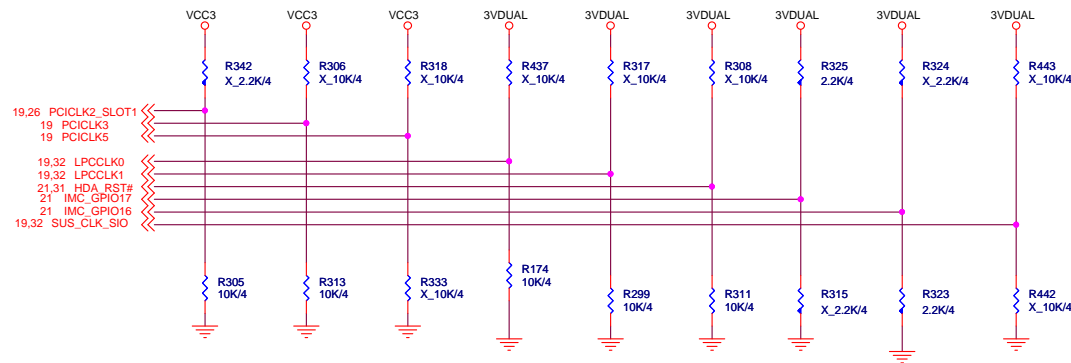






## REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	RESERVED	ROM TYPE: H, H = Reserved H, L = SPI ROM    DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT		L, H = LPC ROM L, L = FWH ROM	

R325 and R323 have been changed from 10K ohm to 2.2K ohm 2007/08/01 (AMD demo schematic update)

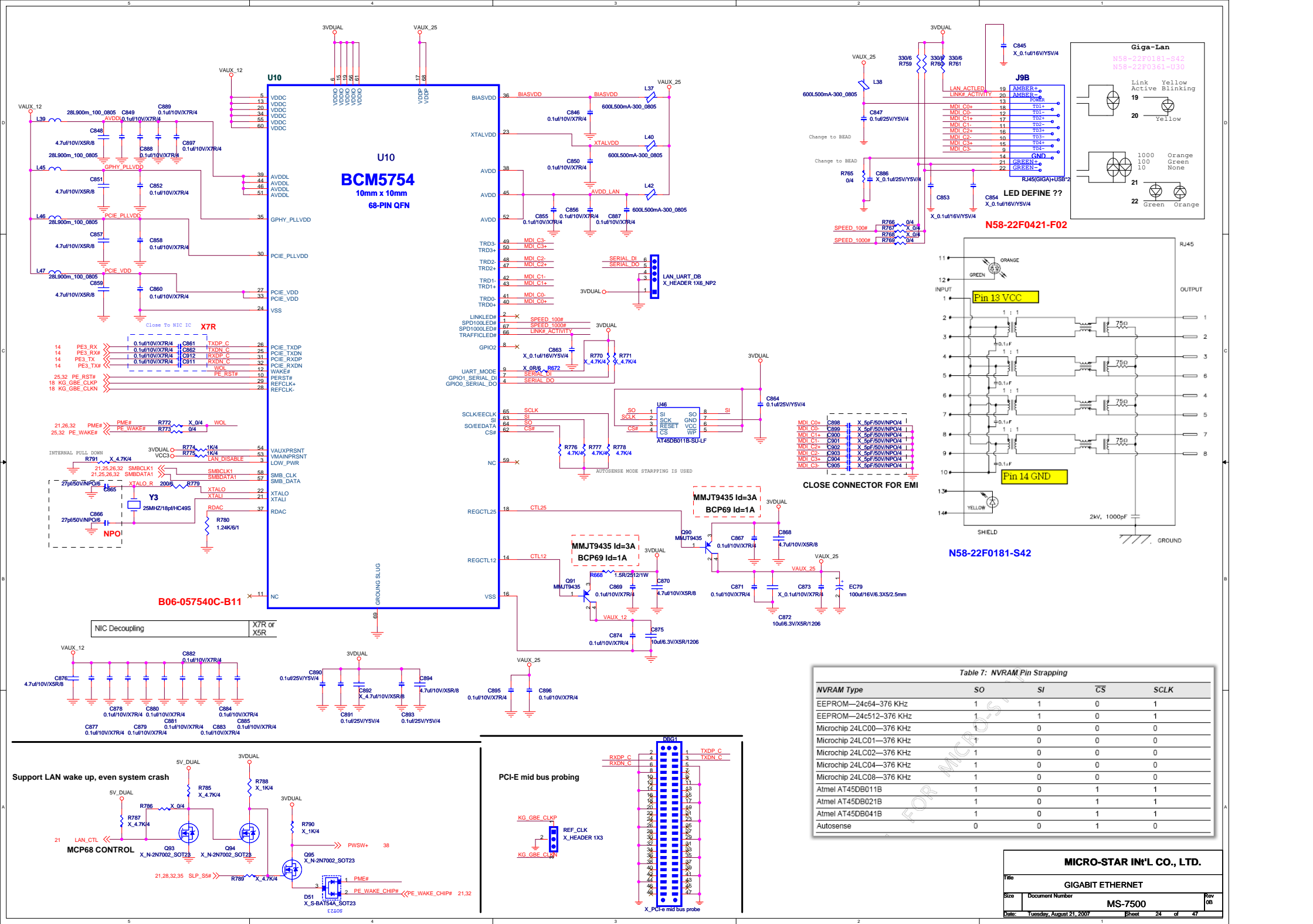
## DEBUG STRAPS

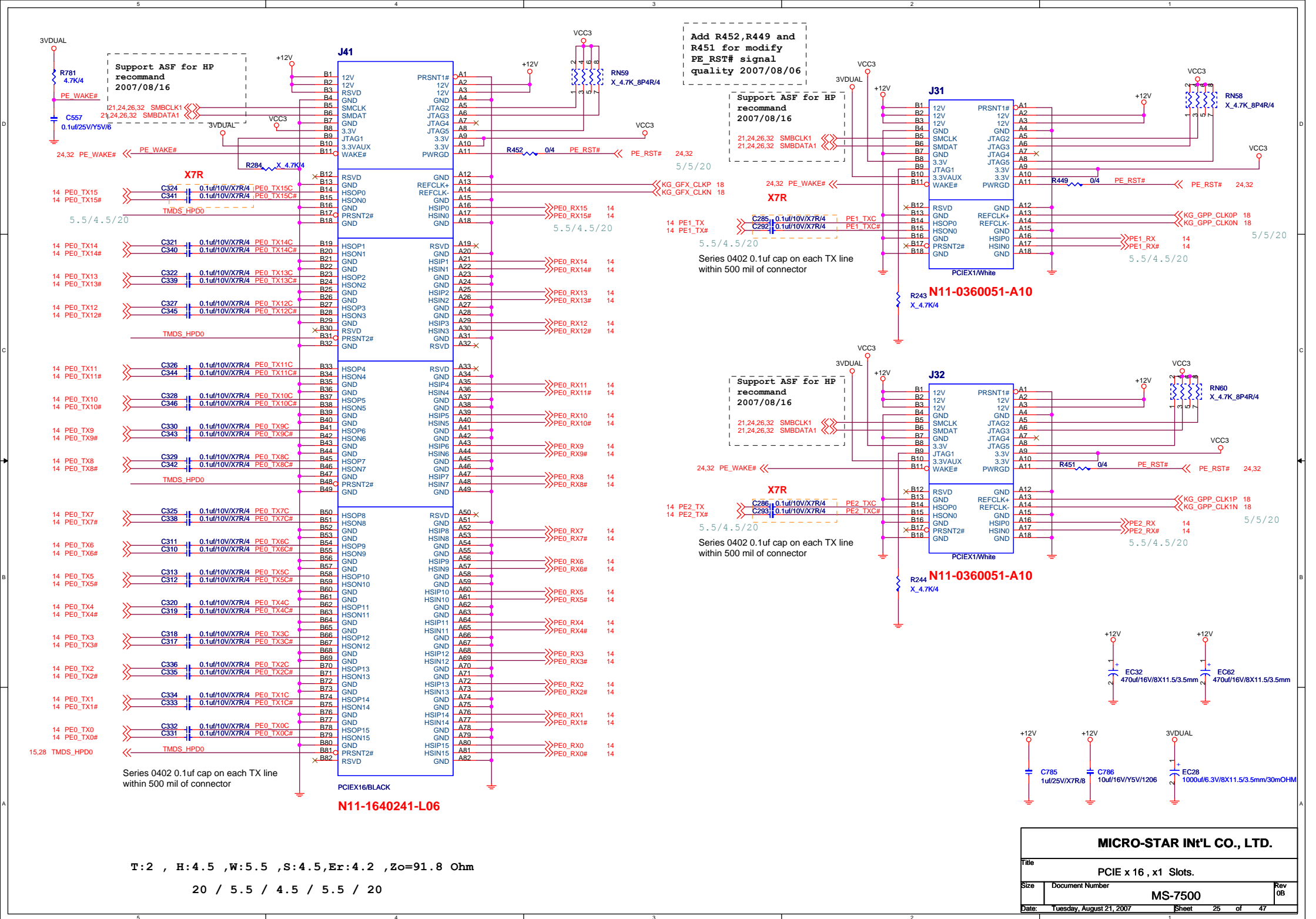
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

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File			
SB700-STRAPS			
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VCC3

E14  
D1x2-BK

E14\_X1  
YJUMPER-MB

R146  
10K/4

R359  
1K/4

ROM\_TBL# 20

VCC3

R803  
6.8K/4

E1

D1x2-BK

R438 1K/4

FDO

20

**J20**

**Pinout Details:**

- Power/Ground:** -12V, +12V, VCC5, VCC3, 3V3V, GND.
- Control/Status:** TRST#, TMS, TDI, INTA#, INT#, PRSNT#1, PRSNT#2, PRSNT#4, REQ#, RS#, GNT#, PME#, IDSEL, FRAME#, TRDY#, STOP#, SDONE, SBO#, PAR, AD14, AD13, AD11, AD9, X2, C/BE#0, REQ64#A.
- Data/Address:** PCI\_INT#, PCI\_INTH#, PCI\_CLK2\_SLOT1, PCI\_REQ0#, C\_BE#3, C\_BE#2, IRDY#, DEVSEL#, PCI\_LOCK#, PERR#, SERR#, C\_BE#1, ACK64#, X1, X2, C\_BE#0, REQ64#A.

**Support recommendation**  
2007/08/

VCC5

C370 0.1µF/25V/Y5V4  
C402 0.1µF/25V/Y5V4  
C385 0.1µF/25V/Y5V4

VCC3

C386 0.1µF/25V/Y5V4  
C401 0.1µF/25V/Y5V4  
C403 0.1µF/25V/Y5V4

3VDUAL

C399 0.1µF/25V/Y5V4  
C369 0.1µF/25V/Y5V4

**CPU**

**RN47**  
X 8.2K 8P4/R4

DEVSEL# 6 7  
TRDY# 4 5  
IRDY# 4 3  
FRAME# 2 1

**RN43**  
X 8.2K 8P4/R4

STOP# 2 1  
PCI LOCK# 4 3  
PERR# 6 5  
SERR# 8 7

ACK6# R326 8.2K/4  
REQ6# R303 8.2K/4

VCC3

Title			
PCI Slot1			
Size	Document Number		Rev
	MS-7500		0B
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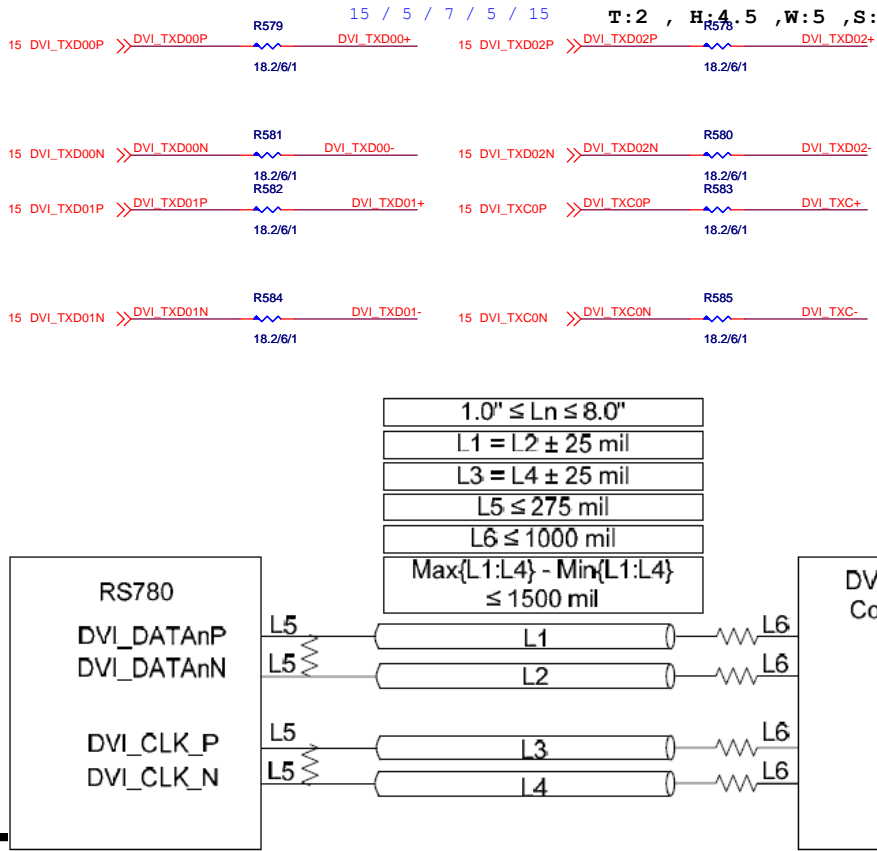
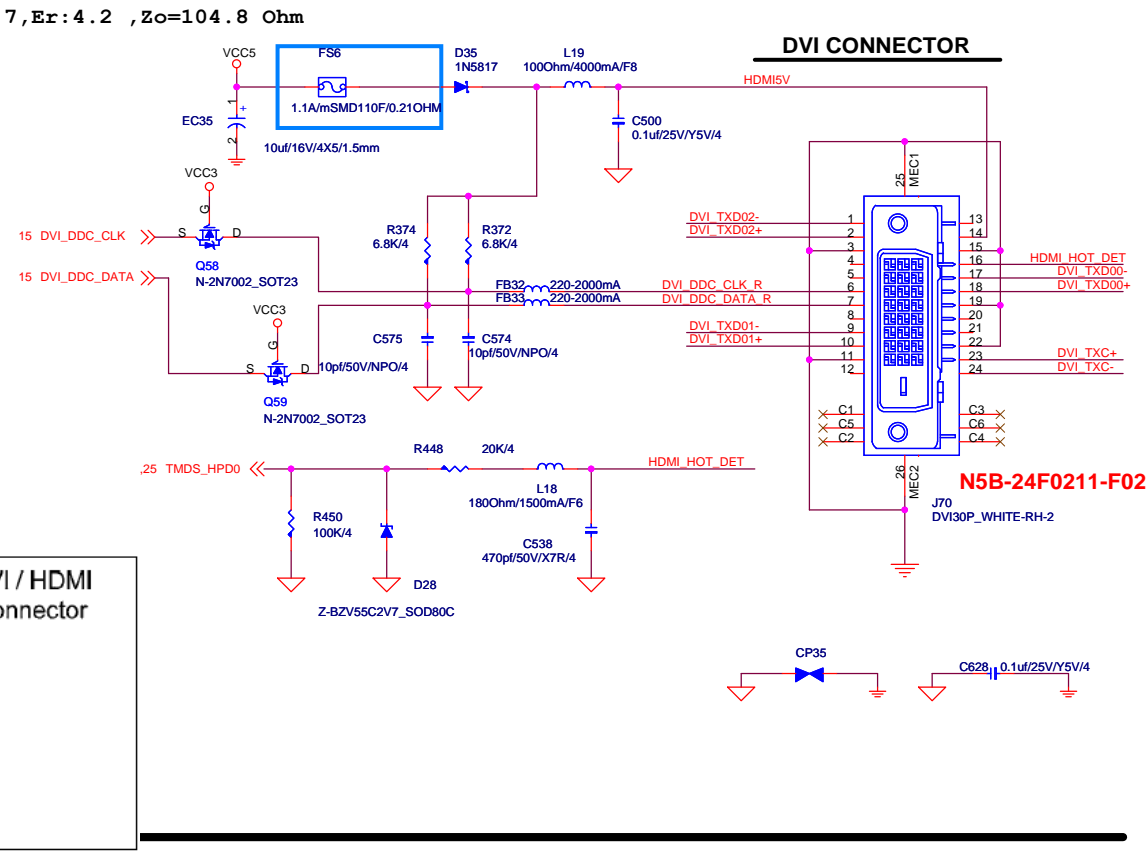
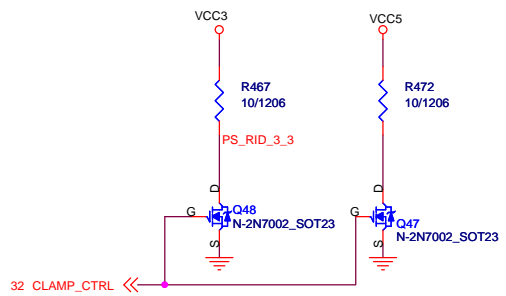


Figure 32: Layout Guidelines for the DVI/HDMI Signals

7.1.6 Residual Voltage Bleed-Off Circuit

A residual voltage circuit is required on the board. This circuit must be active in the S3, S4, and S5 state, whenever the main +5 V and +3.3 V power are turned off. A circuit diagram is shown below. When the system is in S3, S4, or S5, the transistors will be turned on, which will clamp any residual voltage on +5V and +3.3 V to ground. See the figure below for an example of a bleed-off circuit.

BLEED-OFF CIRCUIT



MEMORY VOLTAGE BLEED-OFF CIRCUIT

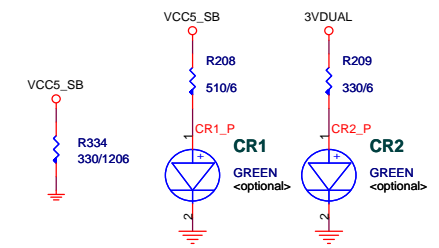
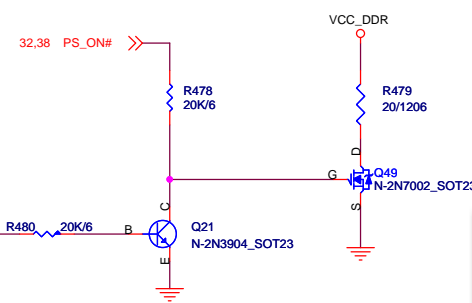
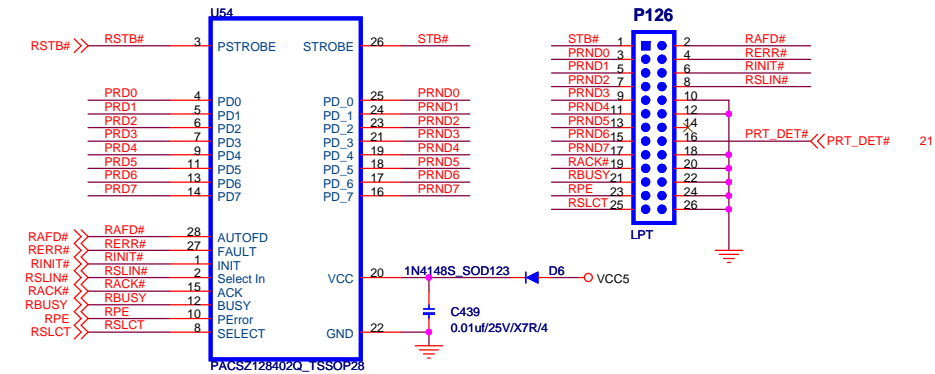


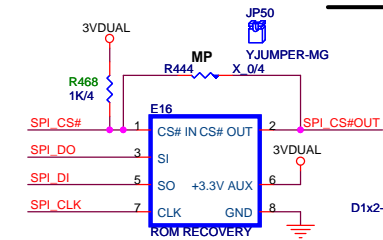
TABLE 38  
SYSTEM BOARD LED REQUIREMENTS

Function	Ref Des	Color
+5 V AUX	CR1	Green
+3 V AUX	CR2	Green

# PARALLAL PORT



# SPI ROM



Connect E16 pin1 and pin2

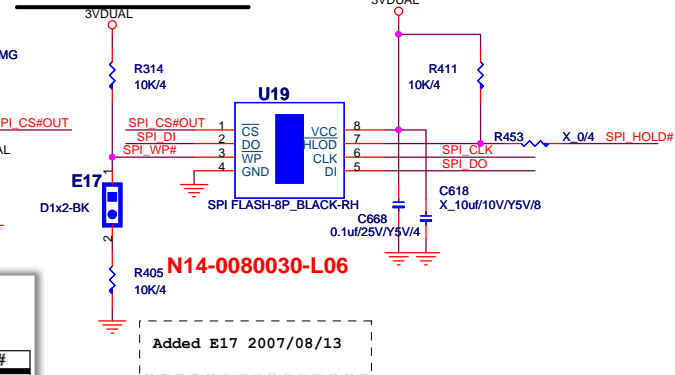


TABLE 22  
ROM RECOVERY HEADER DEFINITION

E16			
PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	CS# IN	CS# OUT	2
3	SI	KEY (no pin)	4
5	SO	VCC (+3.3V AUX)	6
7	CLK	GND	8

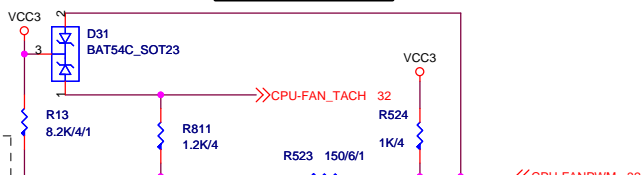
Parallel Port 2 x13 header

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	PE	LDT_RST#	24
	SLCT	GND	26

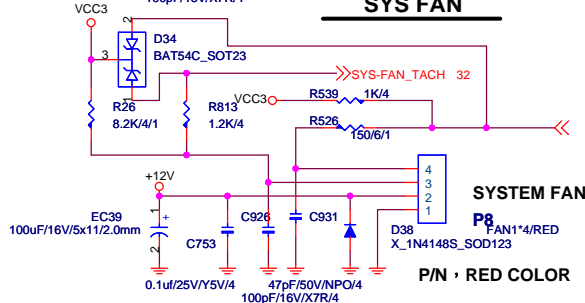
# FAN BOLCK

Modify Fan-circuit for HP reccomand 2007/08/06

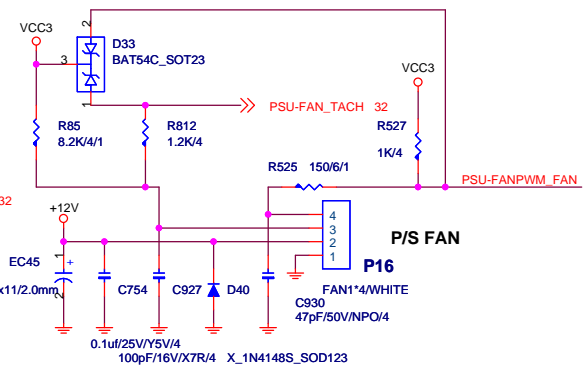
# CPU FAN



# SYS FAN



# PSU FAN



P70 – CPU P8 – Chassis P16 – Power Supply	
Pin #	Signal Name
1	GND
2	+12 V
3	FAN TACH
4	FAN PWM INPUT

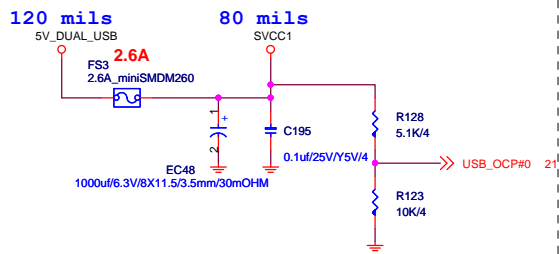
# MICRO-STAR IN'L CO., LTD.

SPI ROM / FAN / LPT		
Size	Document Number	Rev
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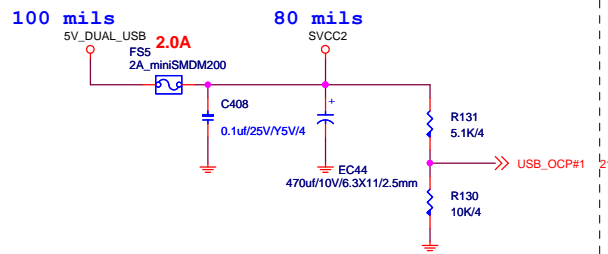
Modify FAN-PWM duty cycle inverter circuit for HP reccomand 2007/08/13



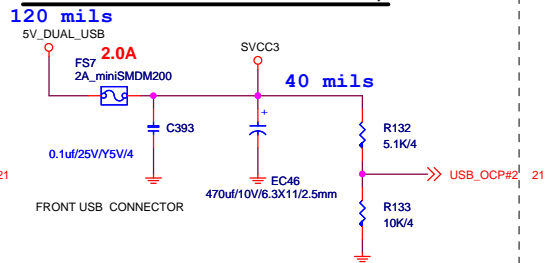
## POWER CIRCUIT FOR USB PORT 0,1,2,3



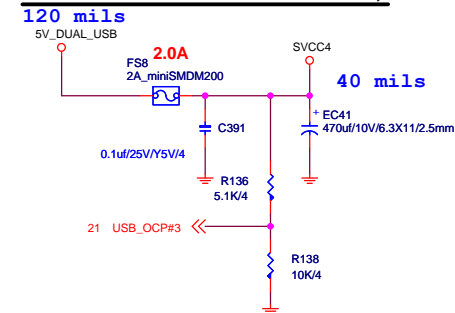
## POWER CIRCUIT FOR USB PORT 4,5



## POWER CIRCUIT FOR USB PORT 6,7

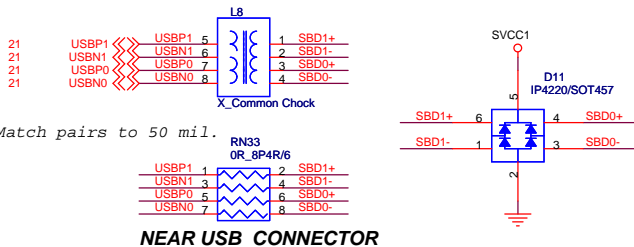


## POWER CIRCUIT FOR USB PORT 8,9



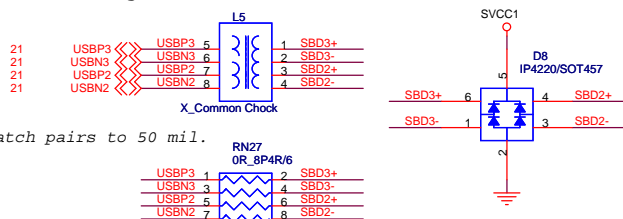
## REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3

Trace lengths must be less 12 inches



NEAR USB CONNECTOR

Trace lengths must be less 12 inches

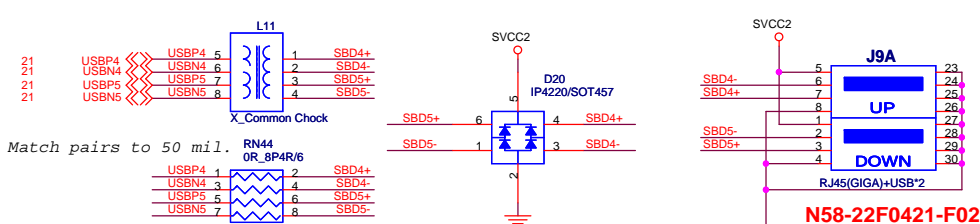


NEAR USB CONNECTOR

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm  
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

## REAL USB CONNECTOR WITH RJ45 FOR USB PORT 4,5

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

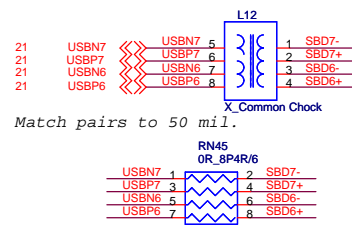
T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm  
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

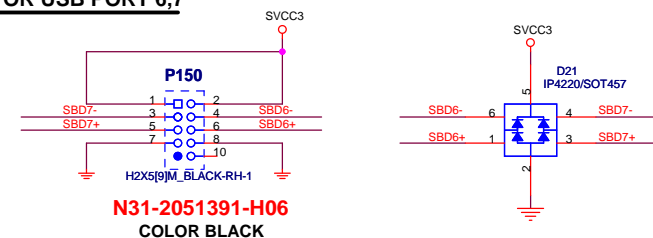
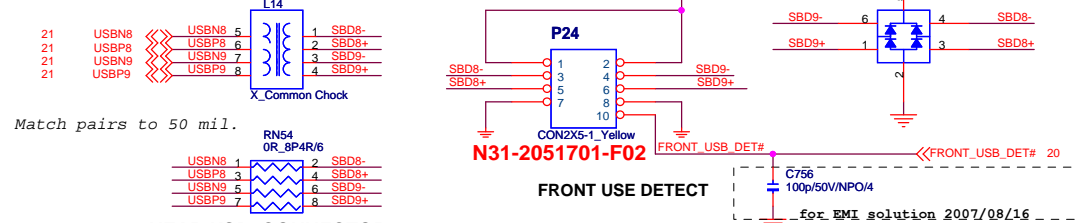


TABLE 10  
MEDIA CARD READER USB HEADER DEFINITION (TOP VIEW)

P150			
Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 4 (-)	USB Port 5 (-)	4
5	USB Port 4 (+)	USB Port 5 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	No Connect	10

## FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

TABLE 9  
FRONT I/O USB HEADER DEFINITION (TOP VIEW)

P24			
Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 8 (-)	USB Port 9 (-)	4
5	USB Port 8 (+)	USB Port 9 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	FRONT USB DETECT#	10

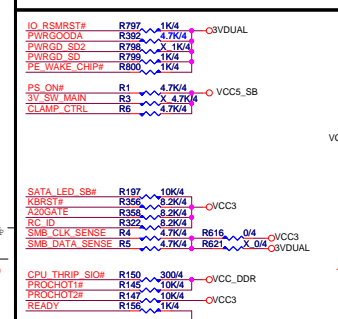
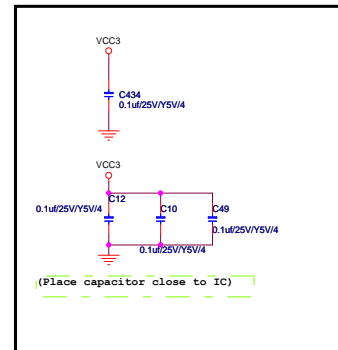
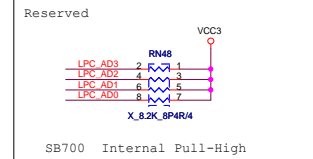
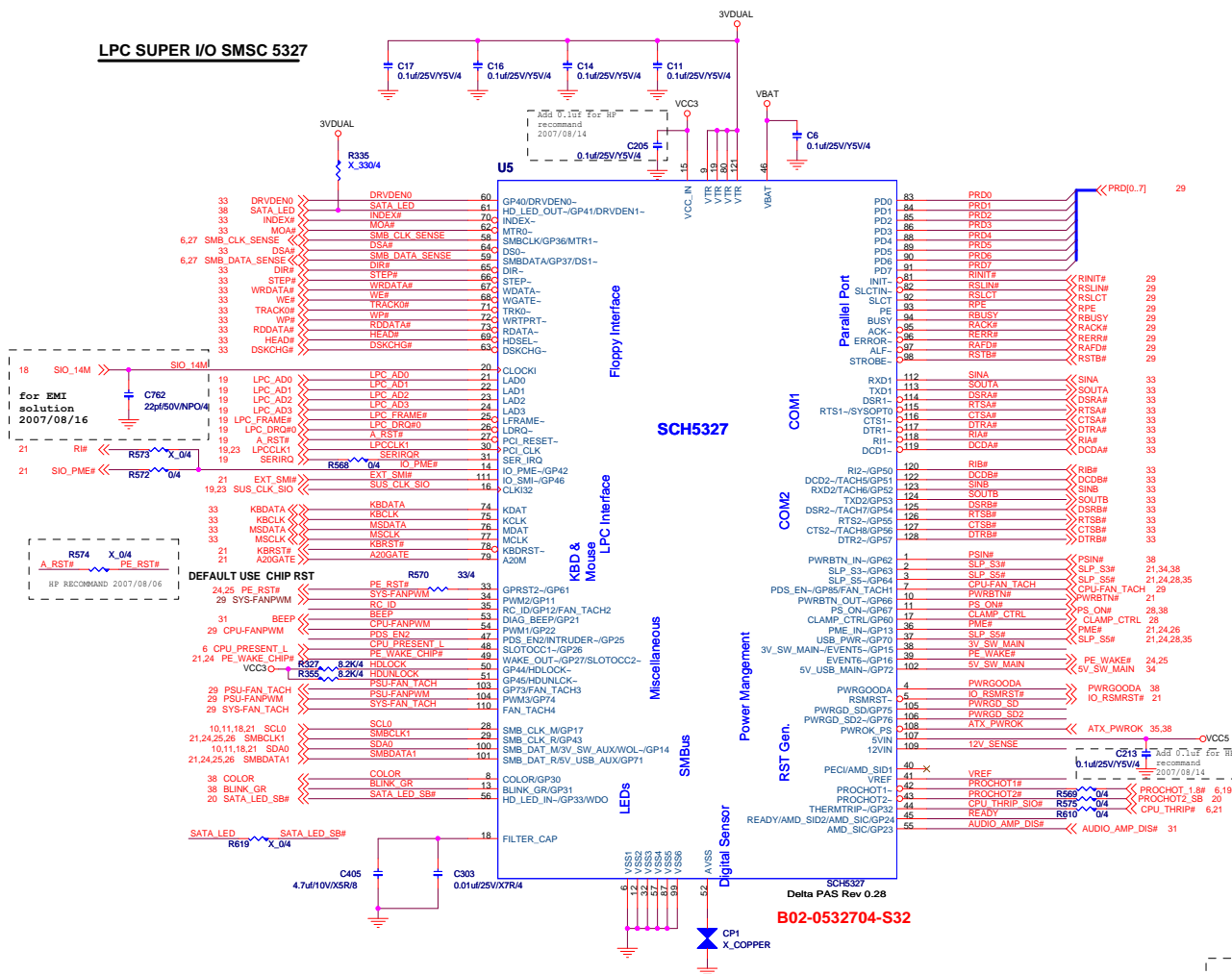
MICRO-STAR IN'L CO., LTD.

USB Conn.			
Size	Document Number	MS-7500	Rev 0B
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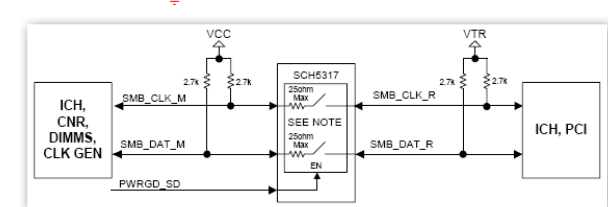
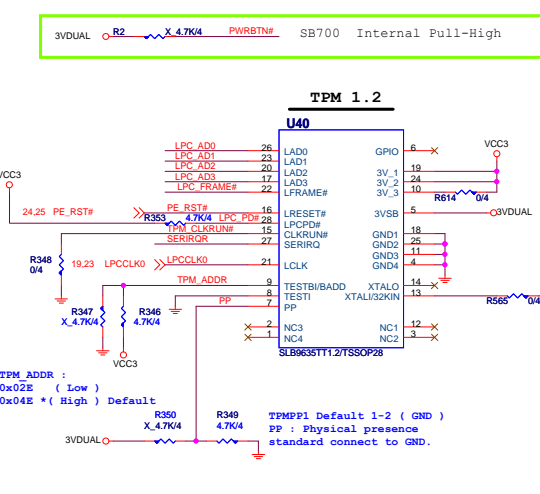
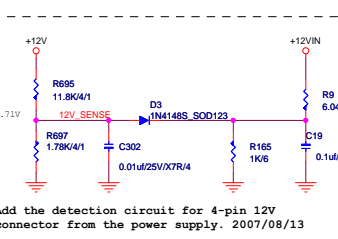


LPC length should be less than 18 inches.

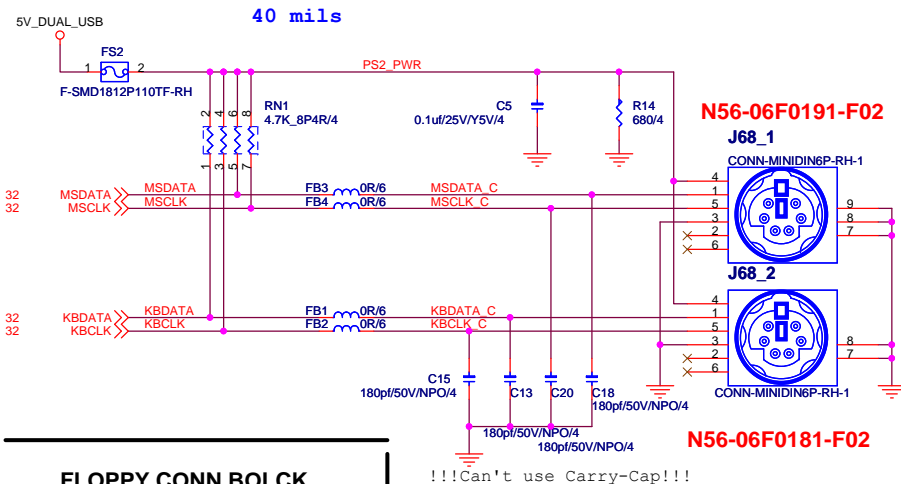
## LPC SUPER I/O SMSC 5327



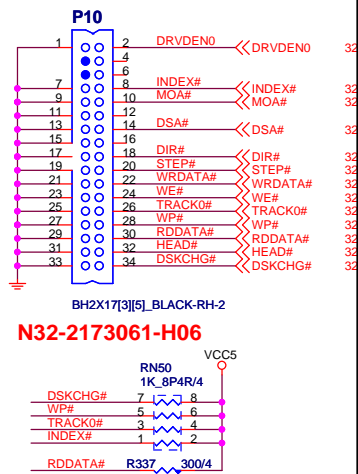
SYSOPT Strap (RTS1-):  
R124 - 0x2E\* DEFAULT  
R144 - 0x4E



## PS2 KEYBOARD & MOUSE CONNECTOR

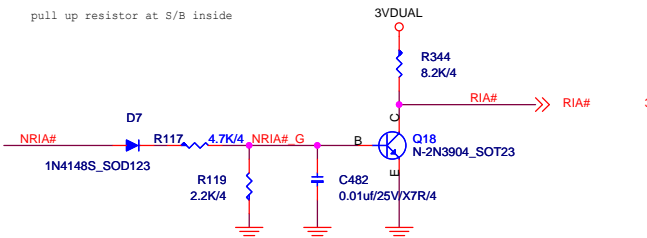


## FLOPPY CONN BOLCK



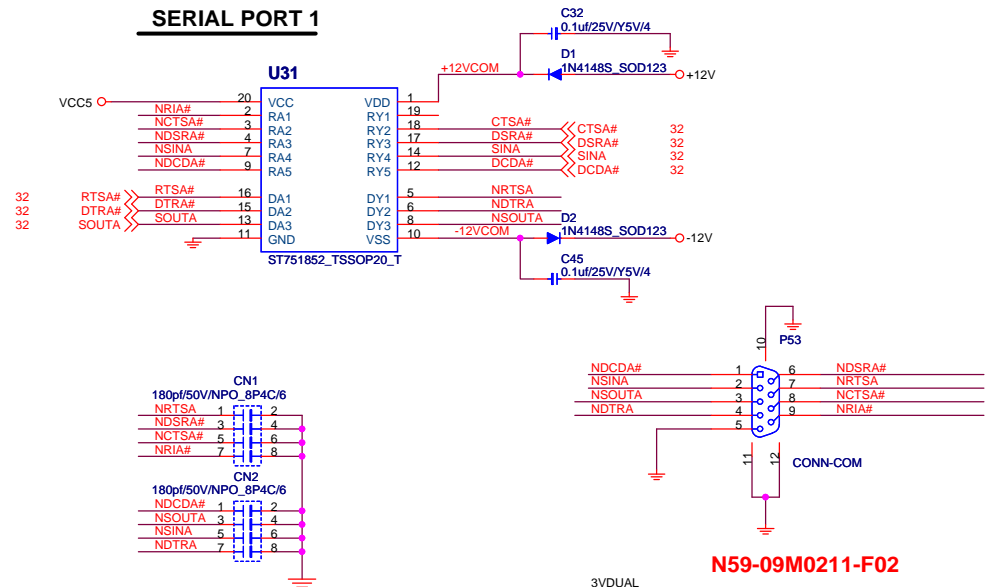
### Support ring wake up

pull up resistor at S/B inside



Modify Ring circuit for HP recommend 2007/08/13

## SERIAL PORT 1



## SERIAL PORT 2

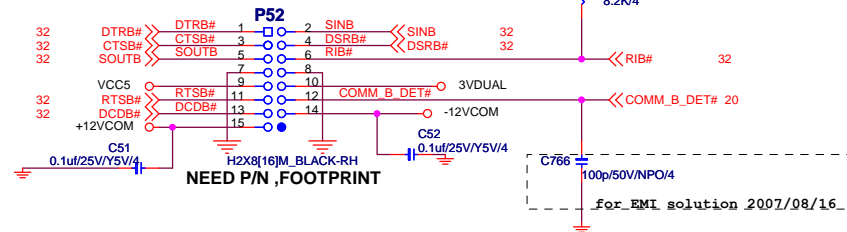
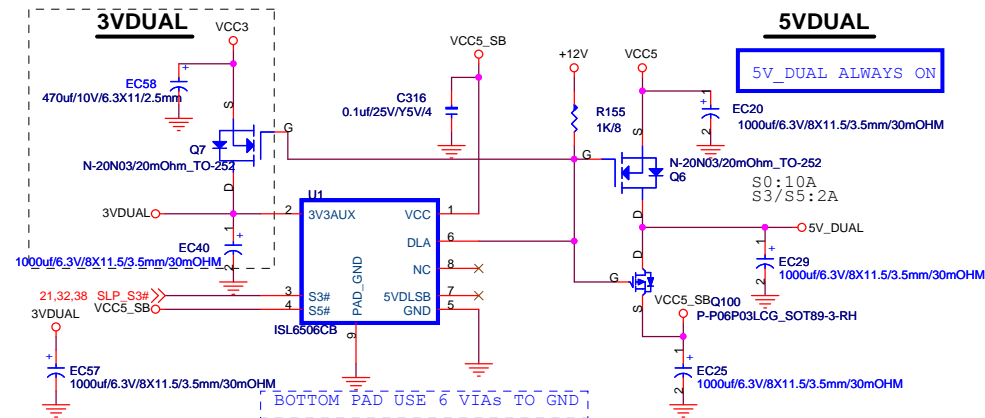


TABLE 12  
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

P52			
Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

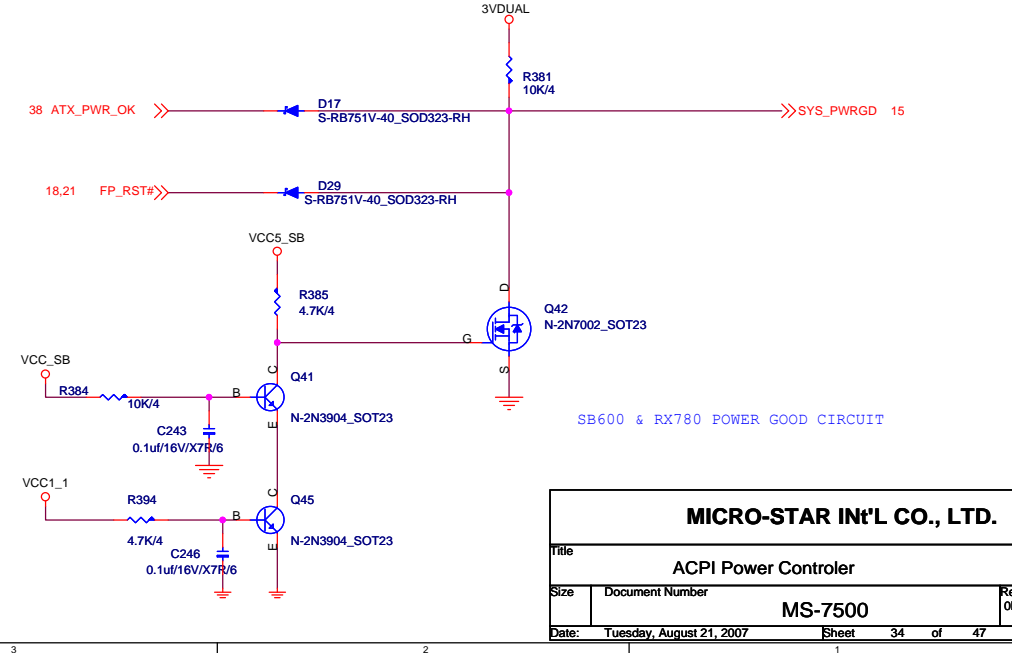
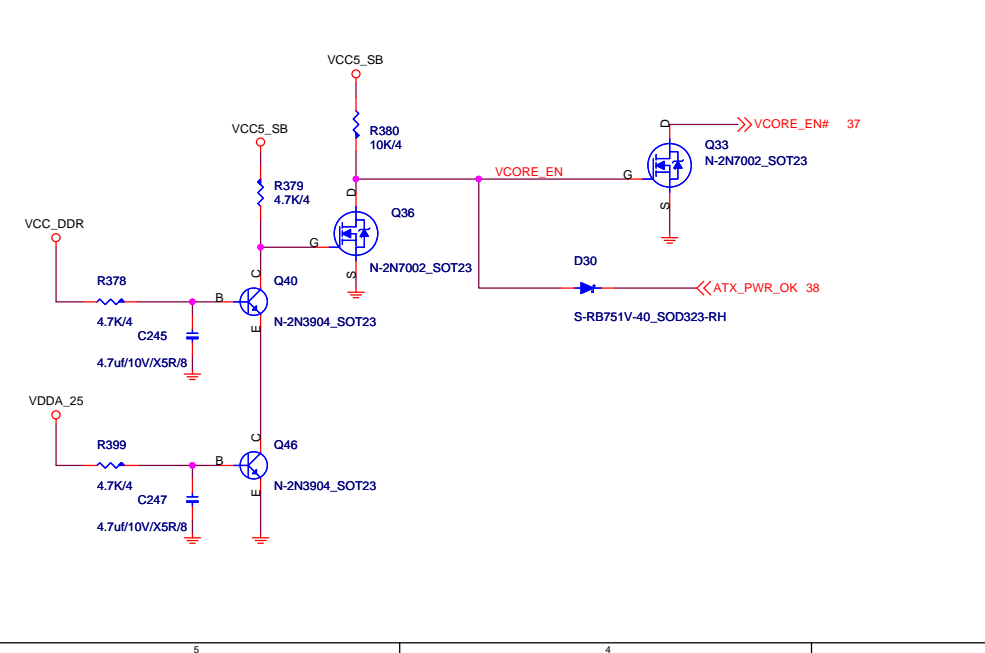
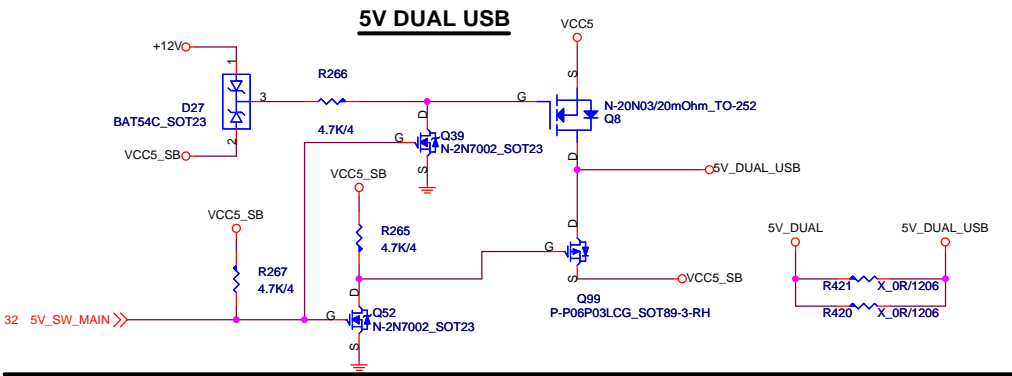
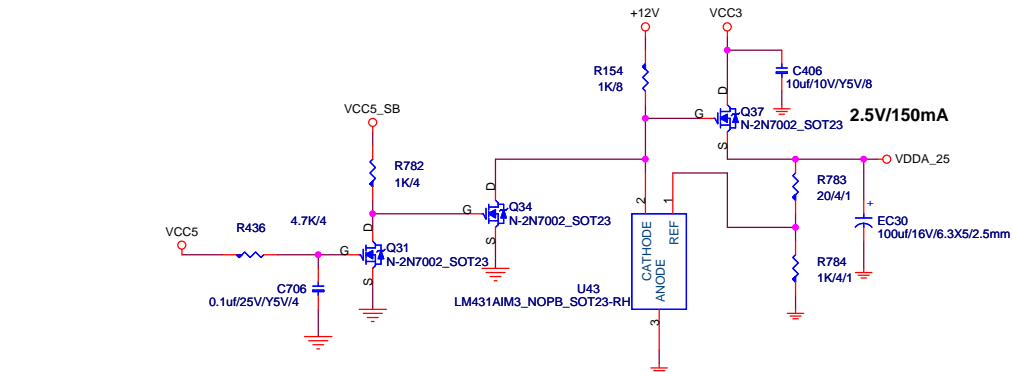
## MICRO-STAR IN'L CO., LTD.

Title			
KB/MS&COM1&Floppy Conn.			
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ACPI POWER STATE SUPPORT

Voltage	S0/S1	S3	S4/S5	S5	No AC
3.3 V Main	On	Off	Off	Off	Off
5 V Main	On	Off	Off	Off	Off
12 V	On	Off	Off	Off	Off
-12 V	On	Off	Off	Off	Off
CPU Core Voltage	On	Off	Off	Off	Off
RS780 core/SB800	On	Off	Off	Off	Off
1.8 V DDR2_VDDQ	On	On	On	Off	Off
0.9 V DDR2_VTT	On	On	On	Off	Off
5 V Standby	On	On	On	On	Off
3.3 V Standby	On	On	On	On	Off
5 V Dual (USB-PS/2)	On - main	On - aux	Off	Off	Off
5 V Dual (Memory)	On - main	On - aux	On - aux	Off	Off
3.3 V Dual (PCI)	On - main	On - aux	On - aux	On - aux	Off
3.3 V LAN (EPW)	On	On	On	On	Off
3.3 V Digital Audio	On	On	Off	Off	Off
5 V Analog Audio	On	Off	Off	Off	Off
Battery/RTC Voltage	On	On	On	On	On



## DDR II 1.8V POWER

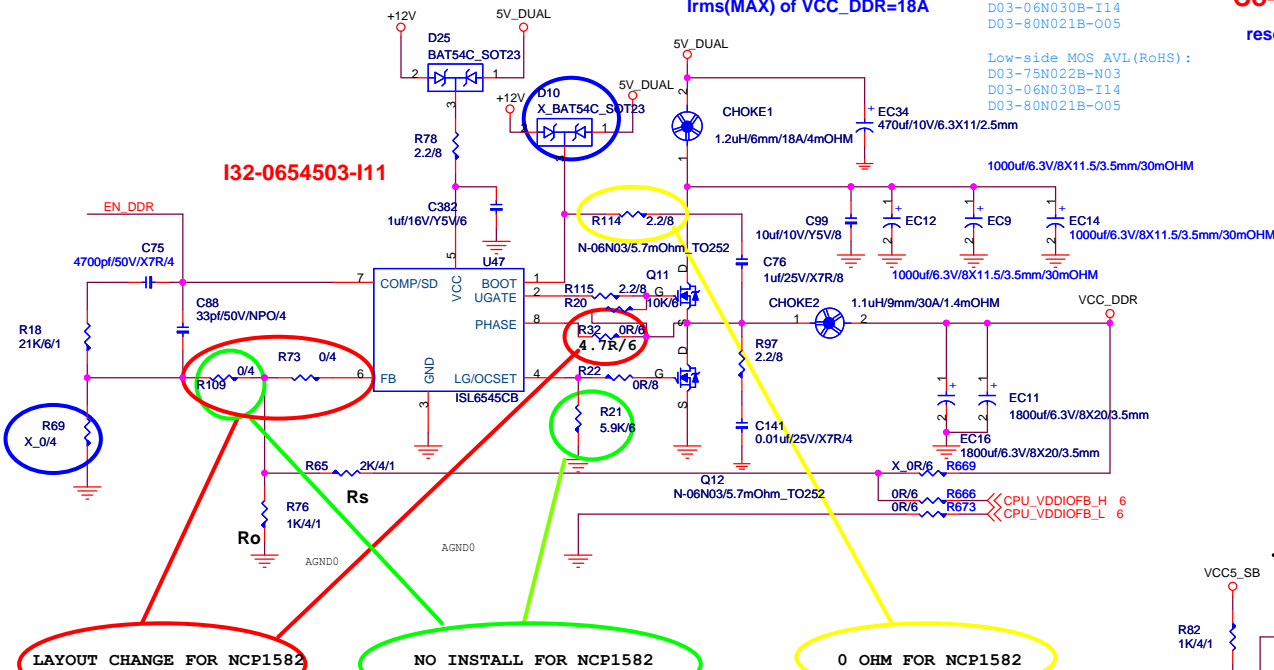
**Irms(MAX) of VCC\_DDR=18A**

## Co-lay ISL6545 and NCP1582A

reserved for NCP1582A

Low-side MOS AVL(RoHS):  
D03-75N022B-N03  
D03-06N030B-I14  
D03-80N021B-O05

**I32-0654503-I11**



LAYOUT CHANGE FOR NCP1582

NO INSTALL FOR NCP1582

0 OHM FOR NCP1582

for Intersil
D10, R69 not install R109 0 ohm R32 0 ohm R114 2.2 ohm R21 5.9K ohm
for ON-semi
D10 BAT54C R109 not install R32 4.7 ohm R114 0 ohm R21 not install R69 0 ohm

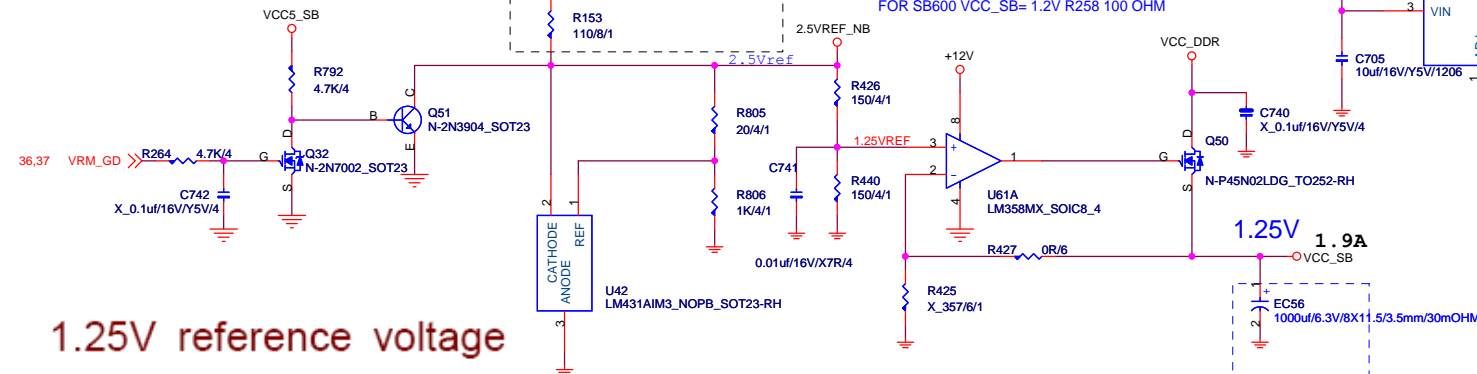
$$I_{PEAK} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where  $I_{OCSET}$  is the internal OCSET current source ( $21.5\mu A$ )

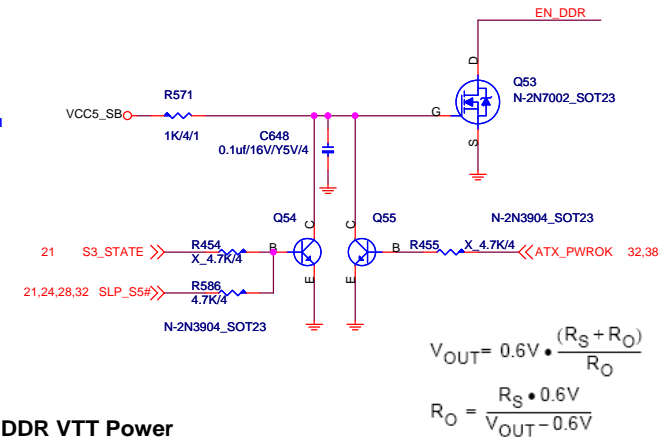
SHUTDOWN CONTROL						
Shutdown Pin Enable Threshold	-	VSD	1.14	1.24	1.34	V

Modify current  
too weak  
2007/08/01

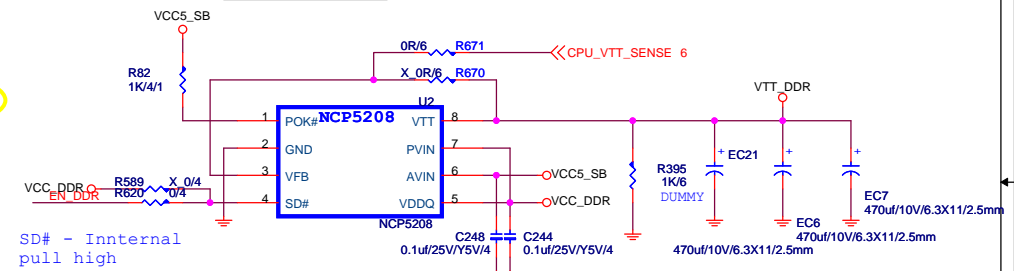
FOR SB600 VCC\_SB= 1.2V R258 100 OHM



1.25V reference voltage


$$V_{OUT} = 0.6V \cdot \frac{(R_S + R_O)}{R_O}$$
$$R_O = \frac{R_S \cdot 0.6V}{V_{OUT} - 0.6V}$$

### DDR VTT Power



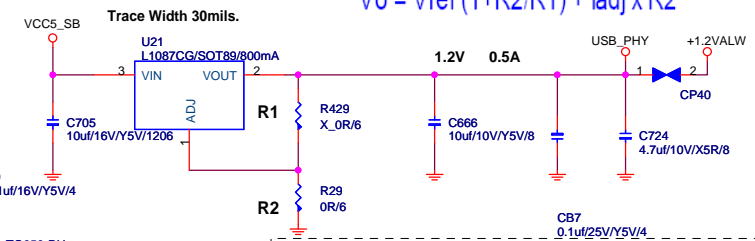
PVIN and GND pin need big power plane

at least 3 vias to inner power plane

**I31-0520803-005**

**I31-0520803-005**

$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$



R429 has been un-populated and R29 has been populated for U21 heat 2007/08/01

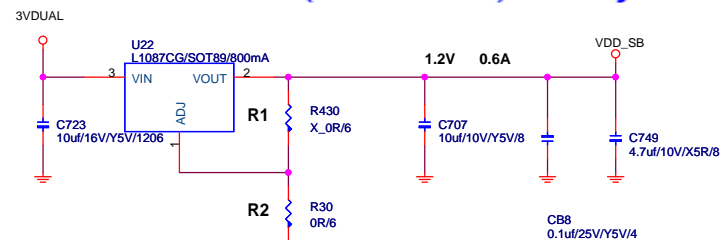
**MICRO-STAR INT'L CO., LTD.**

Title			
Sys. Regulators / DDR			
Size	Document Number	Rev	
	MS-7500	0B	
Date:	Tuesday, August 21, 2007	Sheet	35 of 47



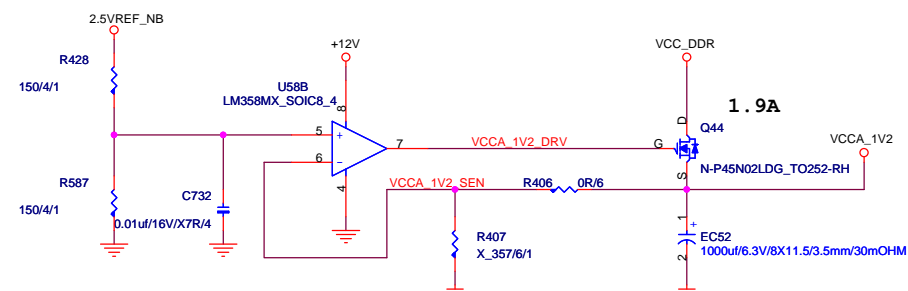
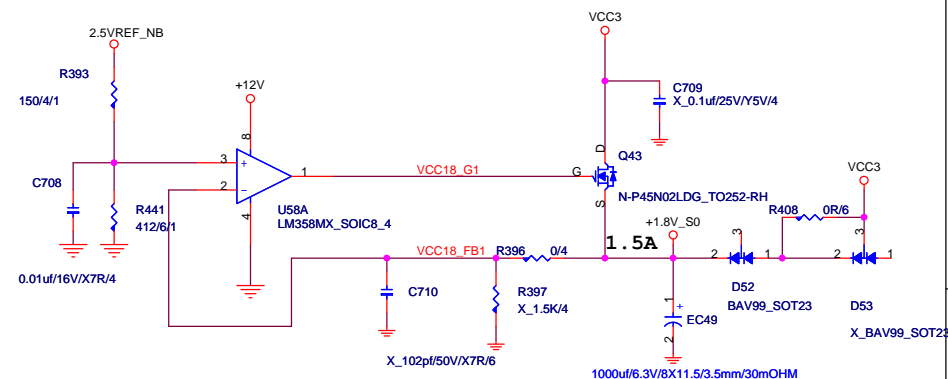
1.25V reference voltage

$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$



PA SB700AA1

R430 has been un-populated and R30 has been populated for U22 heat 2007/08/01

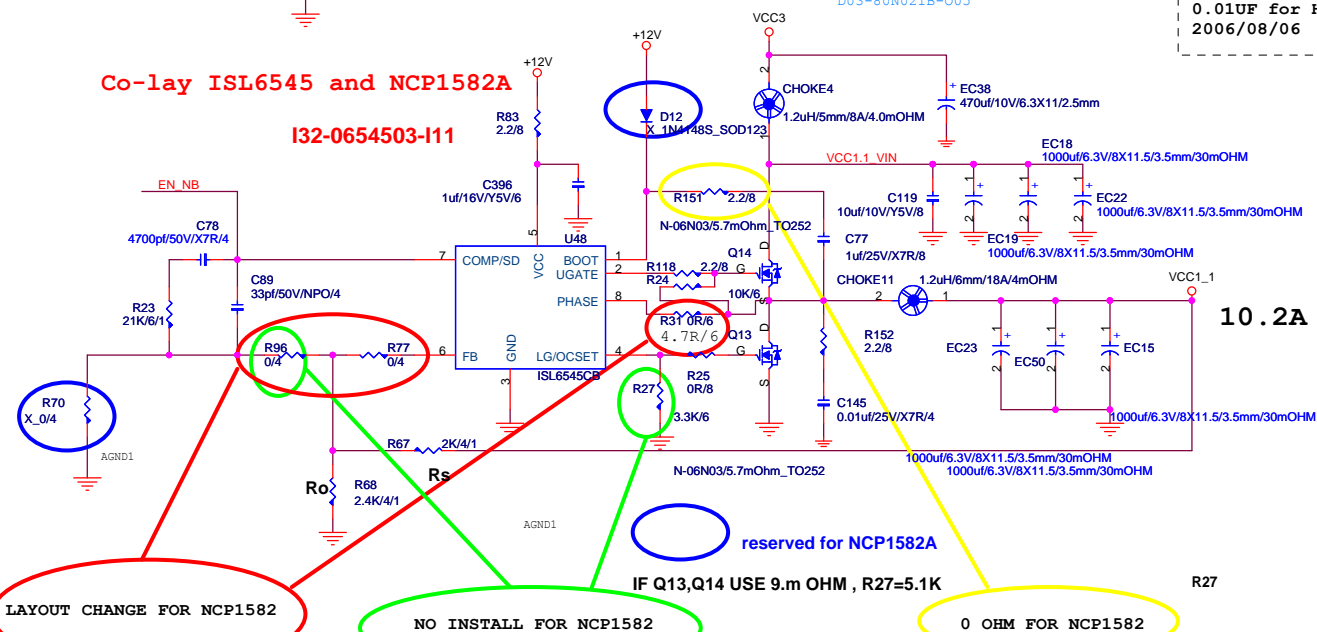


C708 and C732 have been  
change from 0.1UF to  
0.01UF for HP recommand  
2006/08/06

- VLDT Max Current Requirement
  - HT Gen1 - 500mA
  - HT Gen3 - 1.4A

## Co-lay ISL6545 and NCP1582A

**I32-0654503-I11**



$$V_{OUT} = 0.6V \cdot \frac{(R_S + R_O)}{R_O}$$

$$R_O = \frac{R_S \cdot 0.6V}{V_{OUT} - 0.6V}$$

$$I_{\text{PEAK}} = \frac{2 \times I_{\text{OCSET}} \times R_{\text{OCSET}}}{r_{\text{DS(ON)}}$$

where  $I_{OCSET}$  is the internal OCSET current source ( $21.5\mu A$ )

**MICRO-STAR INT'L CO., LTD.**

Title	CORE PWR 1.2/1.1/CPU_HTVDD1.2
-------	-------------------------------

Size	Document Number
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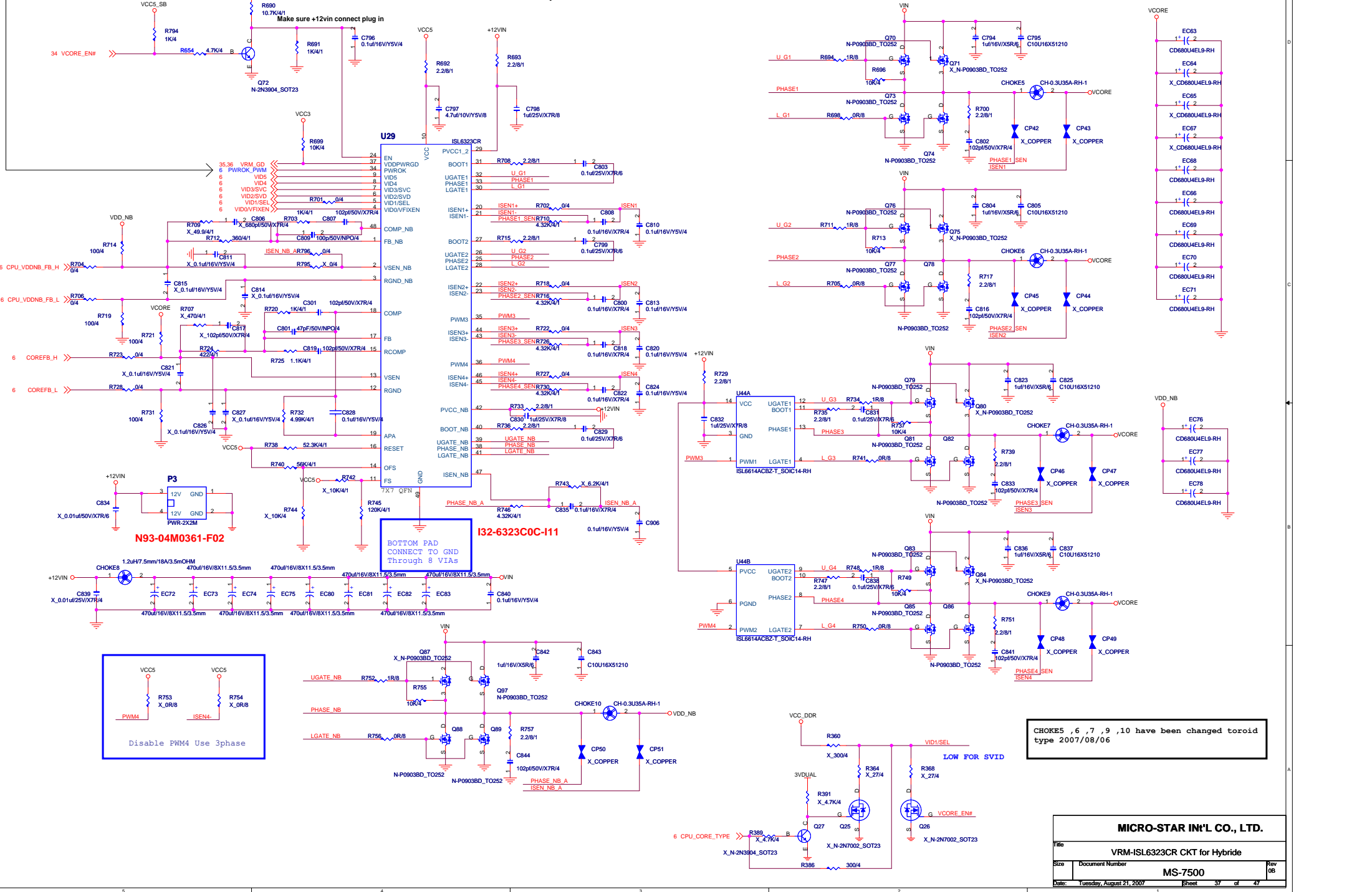
MS-7500

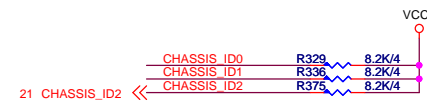
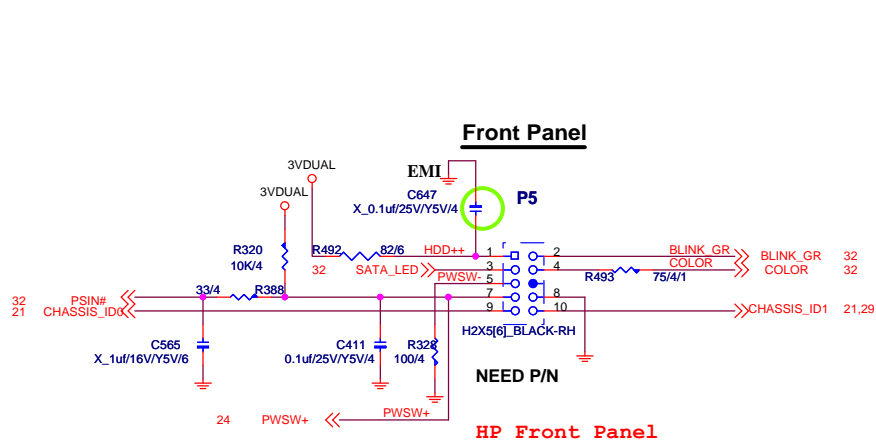
Date: Tuesday, August 21, 2007 Sheet 36 of 4



PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWROK Input HIGH Threshold		2	-	-	V
PWROK Input LOW Threshold		-	-	0.8	V

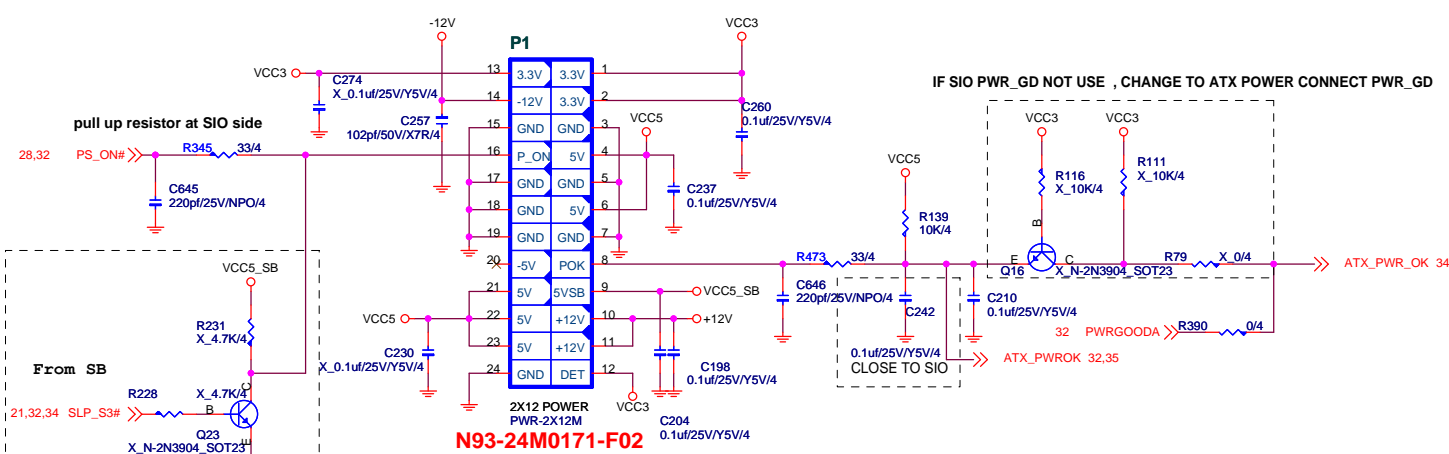
ISL6323CR CKT for Hybride





HD_LED +	1	2	PWR_LED + (BLINK)
HD_LED -	3	4	PWR_LED - (COLOR)
GND	5	6	(key)
POWER_BUTTON#	7	8	GND
CHASSIS_ID0	9	10	CHASSIS_ID1

## ATX Connector



**TABLE 5**

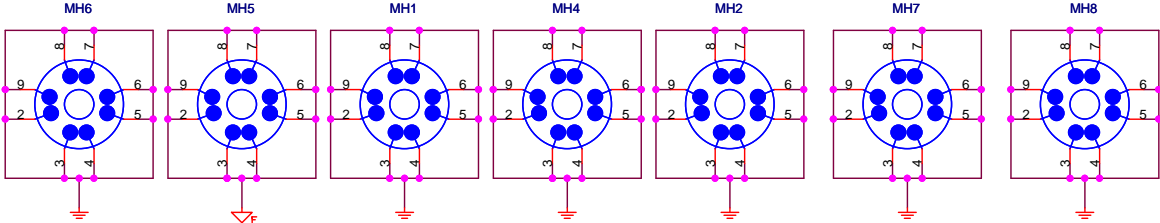
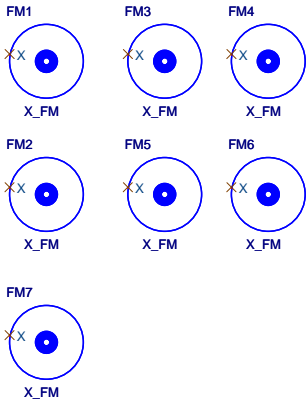
**POWER SUPPLY CONNECTOR PINOUT**

	P1		
+3.3 V	13	1	+3.3 V
-12 V	14	2	+3.3 V
GND	15	3	GND
PSON#	16	4	+5 V
GND	17	5	GND
GND	18	6	+5 V
GND	19	7	GND
NOT USED	20	8	POWER OK
+5 V	21	9	+5 V STANDBY
+5 V	22	10	+12 V
+5 V	23	11	+12 V
GND	24	12	+3.3 V



Optics Orientation Holes

Mounting Holes

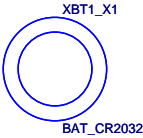
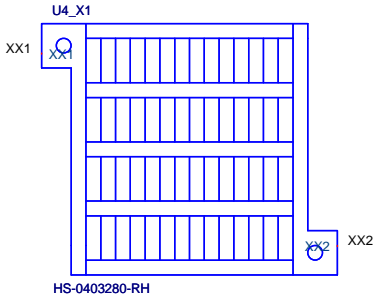
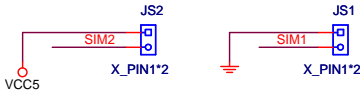


NB/SB FAN/HEAT-SINK

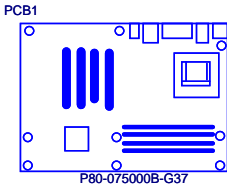
BATTERY

BIOS

Simulation

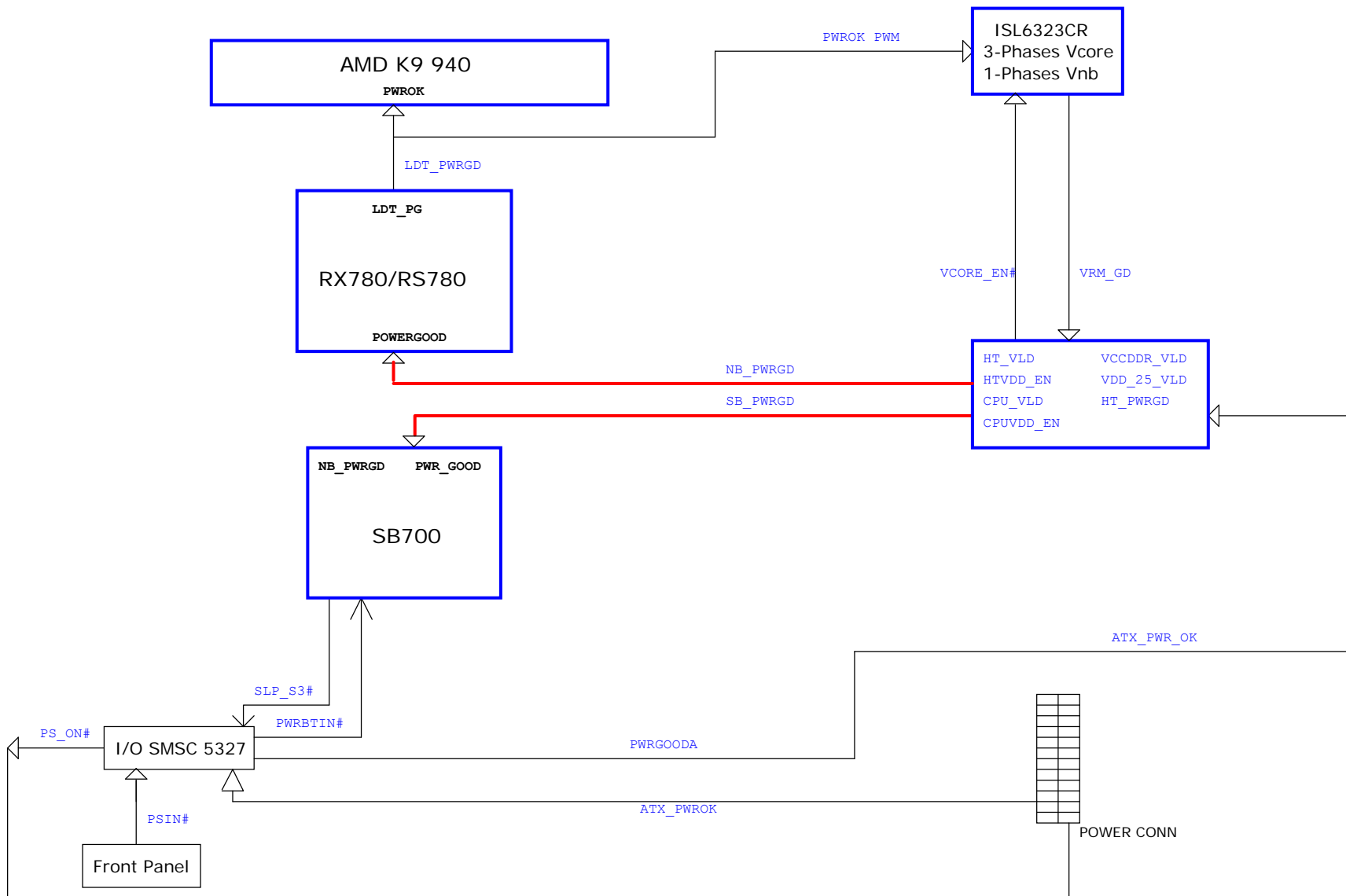


PCB

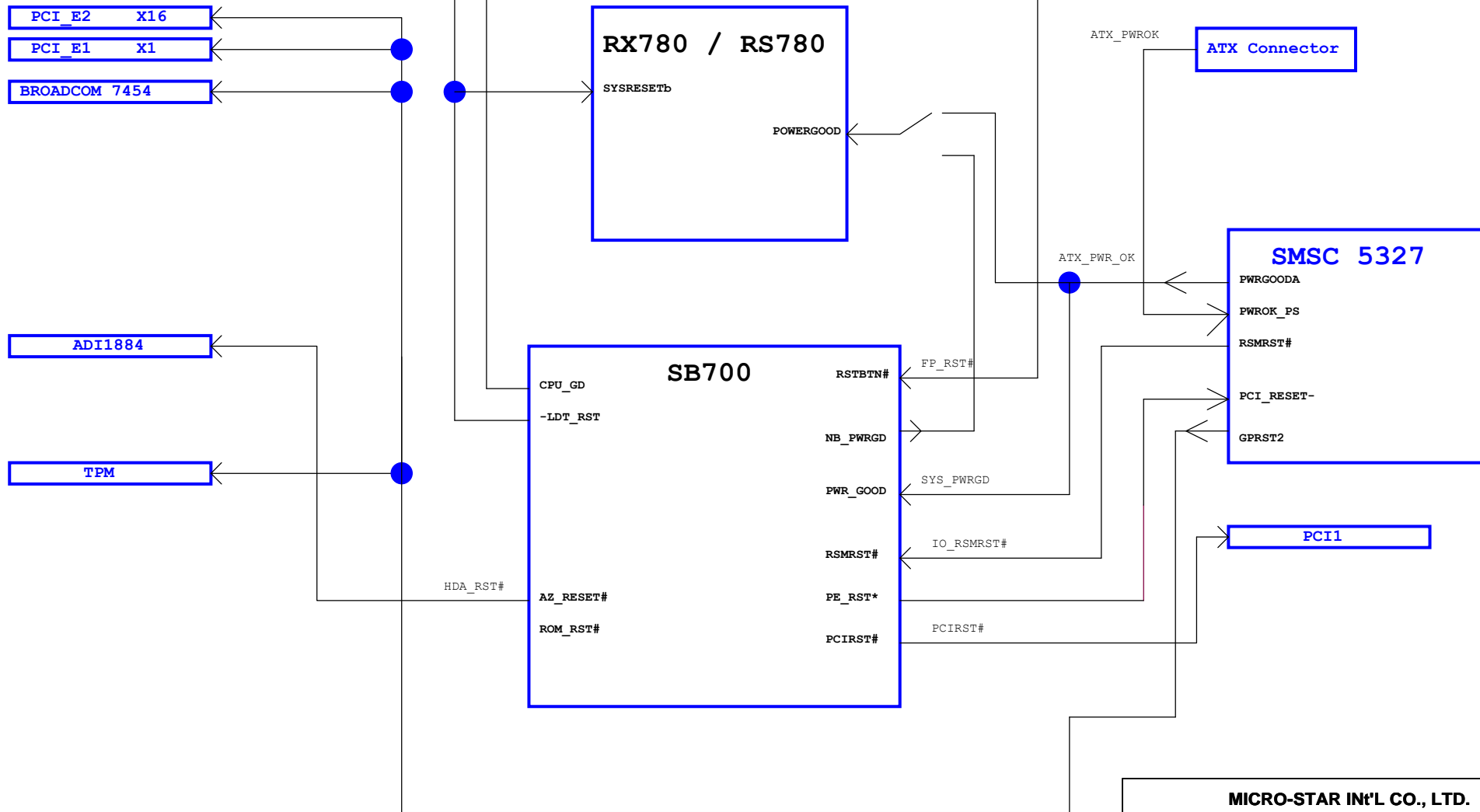


MICRO-STAR INT'L CO., LTD.			
Title			
BOM - Option Parts			
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# PWROK MAP



## RESET MAP



MICRO-STAR INT'L CO., LTD.

Title			
RESET MAP			
Size	Document Number		Rev
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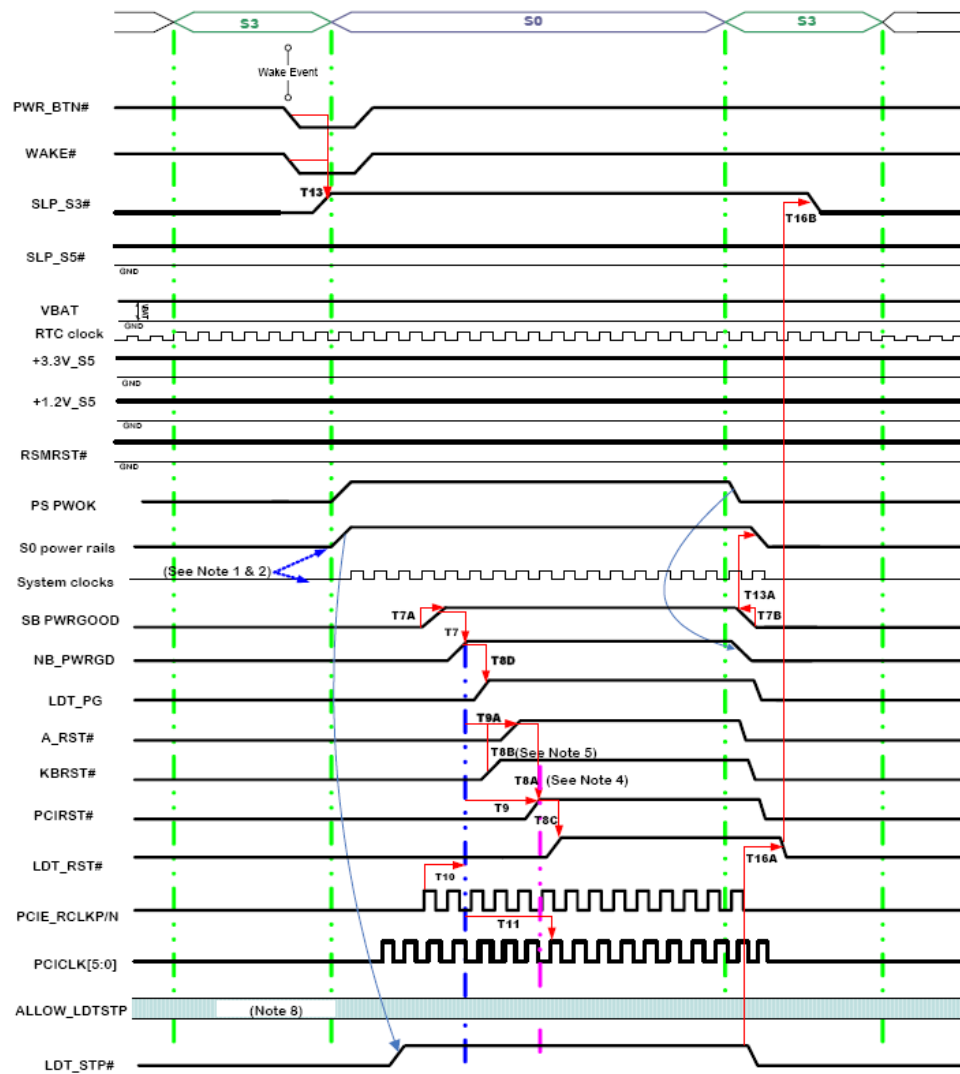


Figure 4-1: SB700 Power Up/Down Sequence

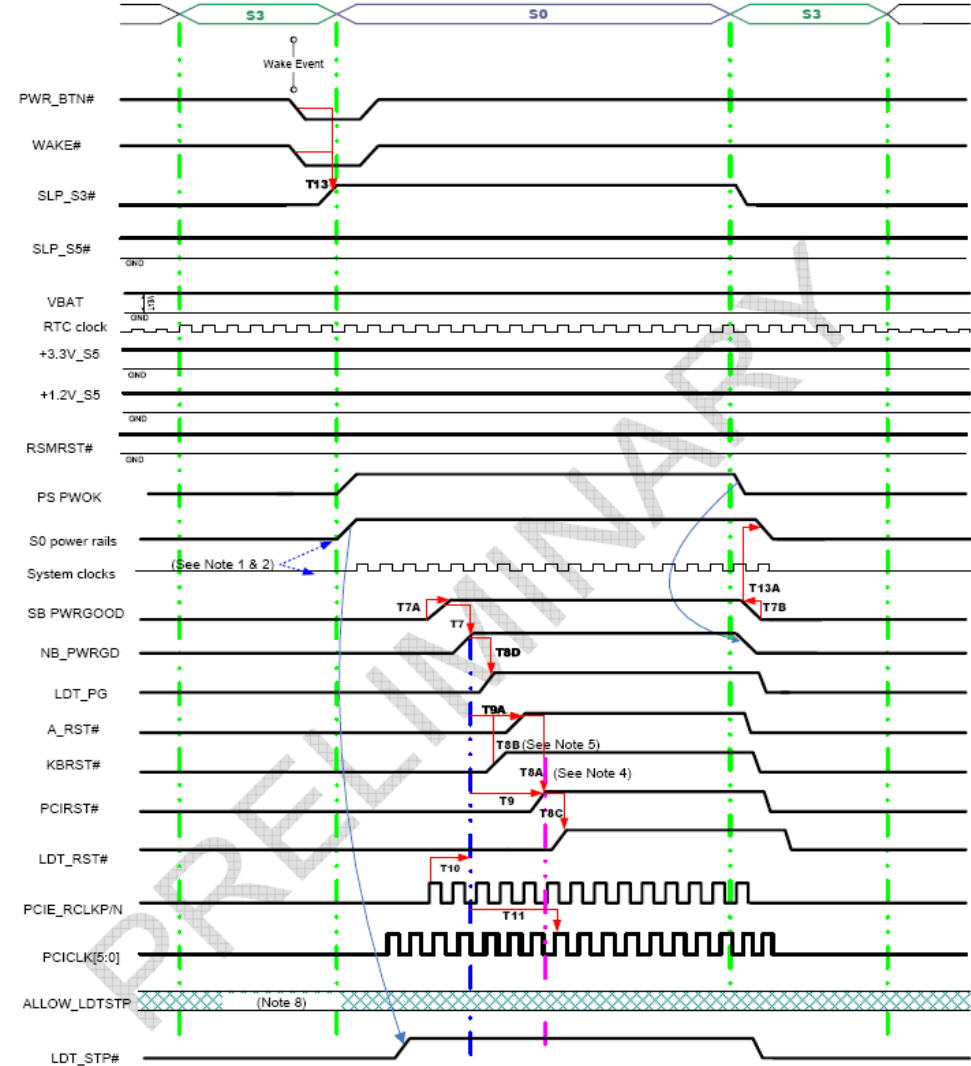


Figure 4-2: SB700 S3/S0 Power Up/Down Sequence



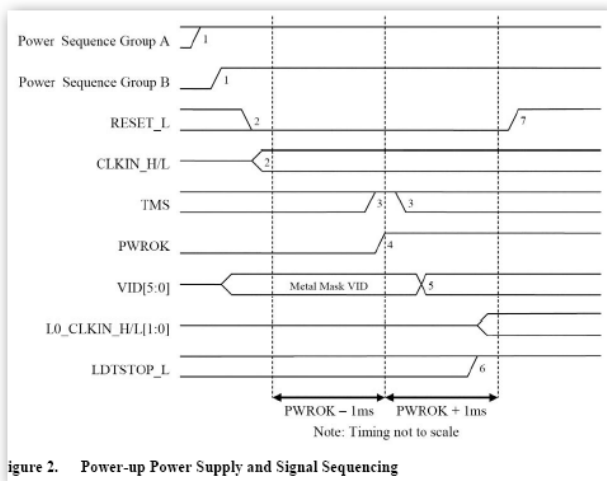


Figure 2. Power-up Power Supply and Signal Sequencing

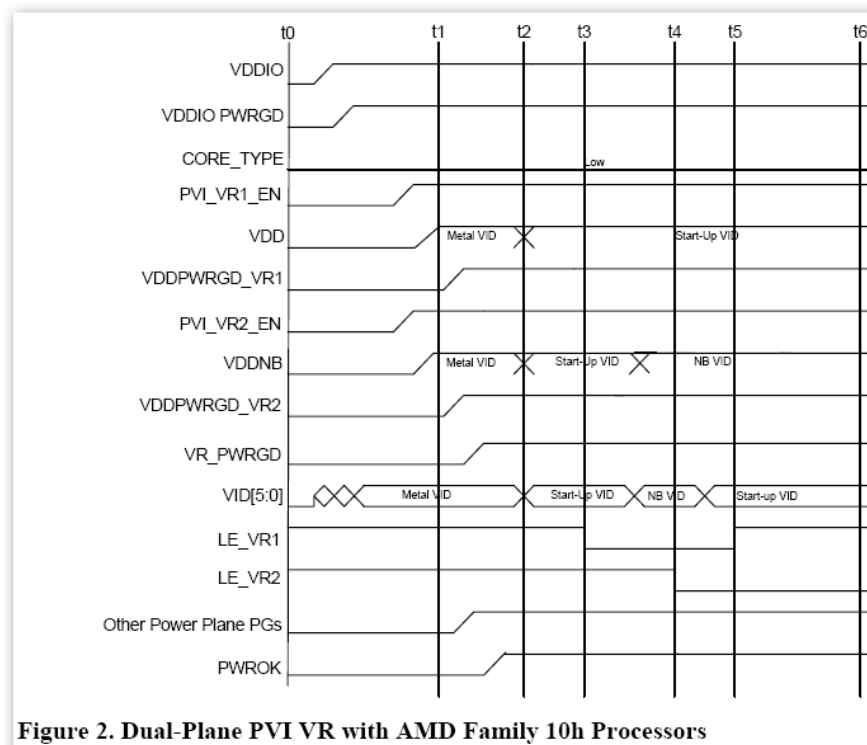


Figure 2. Dual-Plane PVI VR with AMD Family 10h Processors

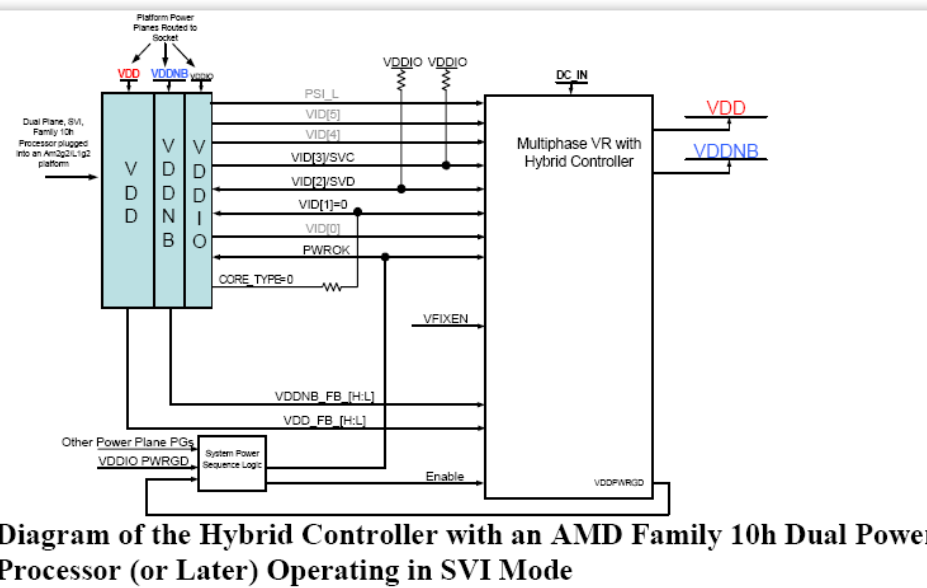


Figure 9. Block Diagram of the Hybrid Controller with an AMD Family 10h Dual Power Plane Processor (or Later) Operating in SVI Mode

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW
12V
+/-5%

2.5V SHUNT  
REGULATOR

VRM SW  
REGULATOR

1.8V VDD SW  
REGULATOR

0.9V VTT\_DDR  
REGULATOR

VCC 1.2V LINEAR  
REGULATOR

VCC 1.1V SW  
REGULATOR

1.8V LINEAR  
REGULATOR

VCC 1.2V LINEAR  
REGULATOR

5V\_DUAL &  
3VDUAL  
REGULATOR ACPI  
CONTROLLER

1.2V STB LDO  
REGULATOR

3.3V LDO  
REGULATOR

LDO  
REGULATOR

BAT

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE	
3.3V	3.0A
12V	5.5A

USB X4 FR	
VDD	
5VDual	2.0A

USB X6 RL	
VDD	
5VDual	3.0A

2XPS/2	
5VDual	1.0A

GBE	
3.3V 0.5A (S0, S1)	
3.3V 0.1A (S3)	

AM2R2
VDDA 2.5V 0.2A
VDDCORE
0.8-1.55V 110A
DDR11 MEM I/F
VTT 1.75A, VDD 10A
VLD1 1.2V 1.4A

RX780/RS780
VDDHT/RX 1.1V 1.2A
VDDHT TX 1.2V 0.5A
VDDPCIE 1.1V 2A
NB CORE VDDC
1.1V 7A
VDDA18PCIE 1.8V 0.9A
PLLs 1.8V 0.1A
VDD18/VDD18_MEM
1.8V 0.01A
VDD_MEM 1.8V 0.5A
AVDD 3.3V 0.135A

SB700
X4 PCI-E 0.8A
ATA I/O 0.5A
ATA PLL 0.01A
PCI-E PVDD 80mA
SB CORE 0.6A
CLOCK
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE I/O 0.2A
3.3V I/O 0.45A

AC97 CODEC
3.3V 59.2 mA
3.3V 31 mA

LAN
3VDUAL 7mA
AVDD1.2V 590mA
AVDD2.5V 235mA

SUPER I/O
3VDUAL 20mA
VCC3 1mA
VBAT 1uA

TPM
3.3V 5mA
3VDUAL 25mA

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06/05/07 Preliminary release

06/15/07

Page 06:R108,R109,R657 AND R658 have been deleted.  
Page 15:C542,C597 AND C745 have been added(FOR EMI).  
Page 15:R93,R126,R165,R190,R199 R201,R167,R204,R270,R255,R179,R222,R236 and R248 have been deleted(using external CLK-GEN)  
Page 15:R175,R179,Q15 and R291 have been added(level-shift for ALLOW\_LDTSTOP).  
Page 15:R197,R45 and R47 have been deleted(DVI single channel).  
Page 18:R338,R339,R340 AND R361 have been deleted(using external CLK-GEN)  
Page 19:R176,R211,R214 AND R215 have been deleted(using external CLK-GEN)  
Page 19:R242 AND R250 have been deleted.  
Page 19:R125 PULLUP 3VDUAL.  
Page 19:Add R276.  
Page 23:R285,R183,R212,R186,R288,R203R,R189,R366,R357,R352,R351and R344 have been deleted(SB700 HAS 15K INTERNAL PULLUP FOR PCI\_AD[30:23])

Page 24:R187,R431,R433 AND R432 have been deleted(using external CLK-GEN)  
Page 25:R408,R409,R394,R402,R414,R415,R410,R424,R430,R422 and R423 have been deleted(using external CLK-GEN)  
Page 28:R625,R626,R627,R628,R629,R630 have been deleted(using DVI single channel)  
Page 31:C771 and C746 have been added(FOR EMI).

06/22/07

Page 06:C157,C158,R99 have been unpopulated,RN3 and R102 have been populated.  
Page 06:U51,RN2 have been deleted(for AMD recommend),R74 and J80 have been added.  
Page 06:Add R183 and Q17(level-shift).  
Page 15:R42,RN43 and Q104 have been deleted,U62 has been added.  
Page 15:R172,R175,R181,R192 and R187 have been changed from 3Kohm to 4.7Kohm.  
Page 15:R182 has been changed from 2Kohm to 10Kohm.  
Page 15:C570 has been changed from 2.2uF to 4.7uF.  
Page 17:Add ferrite bead L18,L26,L27,FB19,FB22.  
Page 18:L10,L13,L16 and L20 have been populated.  
Page 18:C654 and C661have been changed from 10uF to 22uF.  
Page 18:C655 and C733 have been changed from 1uF to 2.2uF.  
Page 15:R161,R223,R230 and R231 been changed from 10Kohm to 8.2Kohm.  
Page 19:R241 has been changed from 5.1Mohm to 20Mohm,R242 has been added.  
Page 19: C323,C354,Y4,R168 have been deleted.U4.J21 connected to GND(25M\_X1).  
Page 20:L29,C412,C924 have been unpopulated.  
Page 21:RN36,RN38,Rn35,RN39,Rn40,C372,C511,C535 and C707 have been deleted,R278,R279 and R280 have been added.  
Page 21:Add R186 and Q22 (level-shift).  
Page 21:SMBDATA1 and SMBCLK1 have been connected U10.  
Page 22:Add C394,C513,C748,L22,L36,L41 and EC84,delete C484,C527,C723.  
Page 22:C489,C717,C734,C735 and C772 have been changed from 10uF to 22uF.  
Page 22:C378,C390,C480,C507,C508,C561,C563,C564,C567,C571,C714,C736,C744 and C747 have been changed from 0.1uF to 1uF.  
Page 22:C392,C510,C527,C528 and C721 have been changed from 1uF to 2.2uF.  
Page 23:R308,R318 and R333 have been unpopulated,R311 have been populated.  
Page 25:Add RN 58,RN59,RN60.  
Page 26:RN43,RN47 have been unpopulated.  
Page 27:R180,R300 have been changed from 3Kohm to 4.7Kohm,and R89,R91 have been changed from 2.2Kohm to 6.8Kohm.  
Page 28:R581~R585,R578~R580 have been changed from 18ohm to 18.2ohm,and R372,R374 have been changed from 2.2Kohm to 6.8Kohm.  
Page 28:L21~L24 have been deleted.  
Page 31:R177 has been changed from 10ohm to 22ohm.

Page 34:Add R394,C246 and Q45 (AMD recommend).  
Page 35:Add R673 (CPU\_VDDIOFB\_L).  
Page 35:Add C723,U22,R430,R30,C707,cb8 and C749 (for PA\_SB700AA1).  
Page 40:Add U4\_X1 (SB HEATSINK).

06/26/07

Page 16:Add R807,R808,C34(for NB MEM\_VREF).  
Page 18:U6 has been changed from ICS9LPRS472 (MLF 64pin) to ICS9LPRS475 (TSSOP 56pin).  
Page 18:R231and R223 have been deleted.  
Page 20:L29 has been deleted and CP14 has been added.

06/27/07

Page 34:C245 has been changed from 0.1uF to 4.7uF.(power sequence)

06/28/07

Page 39:Add C290,C297,C298,C315 for EMI.

06/29/07

Page 15:R173,R135,R574,R196 have been deleted and R189,R190,R196 have been added.  
Page 16:R148,R162,C202 and C203 have been unpopulated.  
Page 19:Add R809,R810,C750,J81 FOR AMD debug.  
Page 21:R125 has been deleted.  
Page 22:C414 has been populated.  
Page 24:R766 and R769 have been populated,R767 and R768 unpopulated. (for HP LAN LED spec)  
Page 27:D44,D45 and D46 pin2 connect to VCC3.  
Page 36:Add D52,D53.

07/04/07

Page 6:R64 has been unpopulated.

07/05/07

Page 34:Add R399,C247,Q46 for S3 function.

07/09/07

Page 13:Adding C920,C925 0.01,uF stitching capacitors for crossing a split when these signals change different reference layer.  
Page 19:Adding C751,C752 0.1,uF stitching capacitors for crossing a split when these signals change different reference layer.  
07/11/07  
Page 21:Added C387 0.1,uF stitching capacitors for crossing a split when these signals change different reference layer.  
Page 32: R575 has been deleted.

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08/01/07

Page 15:Added R93 duo to NC7W207 output pin is op-drain .  
Page 23:R325 and R323 have been changed from 10Kohm to 2.2Kohm. (AMD demo schematic update)  
Page 29:Add R453 because modify SPI\_HOLD# circuit for AMD recommend.  
Page 32 :Modify PS\_IN# circuit for can't boot issue.  
Page 35 :R429 unpopulated and R29 populated for U21 too hot issue.  
Page 36 :R430 unpopulated and R30 populated for U22 too hot issue.  
Page 38 :Modify PS\_ON# and ATX\_PWR\_GD circuit for can't boot issue.

08/07/07

Page 06:Added AMD Sensor Bus for HP recommend.  
Page 15:Added U62.B and R108 for meet powr sequence.

Page 19:Added R248 for 3VDUAL short issue when clean CMOS.  
Page 21:C377 and C373 have been unpopulate for meet power sequence.

Page 21:Added PRT\_DET# circuit..  
Page 25:Added R452,R449 and R451 for modify PE\_RST# signal quality.

Page 27:Added NB THERM circuit for HP recommend.  
Page 29:Modify Fan-circuit for HP recommend.  
Page 32:R335 has been populated for SATA LED.

Page 32:Modify PE\_RST# circuit for HP recommend.  
Page 34:5V DUAL USB circuit have been populated.  
Page 35:R153 has been changed from 220 ohm to 110 ohm for 2.5VREF\_NB voltage isn't stable.

Page 37:CPU PWM circuit follow HOUNDS Ver 0B modified.

08/08/07

Page 29:Added FAN-PWM duty cycle inverter circuit for HP recommend.

08/09/07

Page 6:Added C70 for the voltage divider for the gates of the AMD SB-TSI translation circuit needs a decoupling cap.

Page 27: R592 has been populated and R615 has been un-populated for HP recommend .

08/13/07

Page 13: R34 and R36 have changed to 301 ohm 1% resistor when using RS780 for AMD recommend.

Page 14 and 19:PCI-E signal AC coupling have been changed from Y5V to X7R for AMD recommend.

Page 15: U62 pin5 and R108 pin1 have been connected to 3VDUAL for AMD recommend.

Page 15:Deleted R296. WD\_PWRGD signal only connect to R439.

Page 16: C808 has been changed to 0 ohm when RS780 doesn't use side-port memory for AMD recommend.

Page 17: C598 and C599 has been changed to 0 ohm when RS780 doesn't use side-port memory for AMD recommend.

Page 19:SIO PCICLK has been Changed from PCICLK5 to LPCCCLK1 for AMD recommend.

Page 20: Add R340 .(TEMP\_COMM connect to GND for AMD recommend )

Page 21: Deleted R186 and Q22. (SB THRMTRIP# not Implemented)  
Page 22: C734,C567,C563,C571,C747 have been un-populated when IDE or flash not using for AMD recommend.

Page 25:PCI-E signal AC coupling have been changed from Y5V to X7R for AMD recommend.

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Page 20:R341 and R319 have been un-populated.(SB700 internal pull-up).  
Page 20:Deleted C412 and C924.(SB HW Monitor).  
Page 29:Modify Parall port circuit for HP recommend.  
Page 29:Added E17(SPI Write Protection) for HP recommend.  
Page 29:Modify FAN-PWM duty cycle inverter circuit for HP recommend.  
Page 32:Add the detection circuit for 4-pin 12V connector from the power supply for HP recommend.  
  
Page 33:Modify RING Wake Up circuit for HP recommend.

08/14/07

Page 15:R169 has been changed to 3K ohm and populated for RS780.  
Page 15:R88 and R178 have been populated for RS780.  
Page 15:R198 has been changed to 150 ohm and populated for RS780.  
Page 15:R127 has been populated for RS780.  
  
Page 21:Add R186,Q22 ,R199 level shift circuit to U4 THERMTRIP# for HP recommend.  
  
Page 27:D39 has been populated for USB ESB protection.  
Page 30:D8,D11,D20,D21,D32,D39 have been populated for USB ESB protection.  
  
Page 31:Add C554 and C569 decouple cap for HP recommend.  
Page 32:R335 has been un-populated for HP recommend.  
Page 32:R144 has been changed to 470 ohm.  
Page 32:U31 has been changed from 75232 to 75185.  
Page 33:Net "RDDATA#"pull up resistance value change to 300 ohm.  
Page 35:R454 and R455 have been un-populated.R586 has been changed to 4.7K ohm and populated.  
  
Page 35:R21 has been changed to 5.9K ohm for MSI POWER TEAM recommend.  
Page 36:R27 has been changed to 5.1K ohm for MSI POWER TEAM recommend.  
Page 38:R228,Q23 and R231 have been un-populated.R345 and C645 populated.

08/16/07

Page 39:Added C372,C365,C354 and C364 for EMI.  
Page 39:Added CP2,CP3,CP5,CP6,CP7,CP8 and CP9 for EMI.

08/20/07

Page 15:R188 and R254 have been uninstalled for RS780.  
Page 21:R217 , R260 and C371 have been deleted.( for I2C signal )  
Page 27:Add L6,L21 and L22 for EMI solution.

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